

computing today

ISSN 0142-7210

AUG 1979

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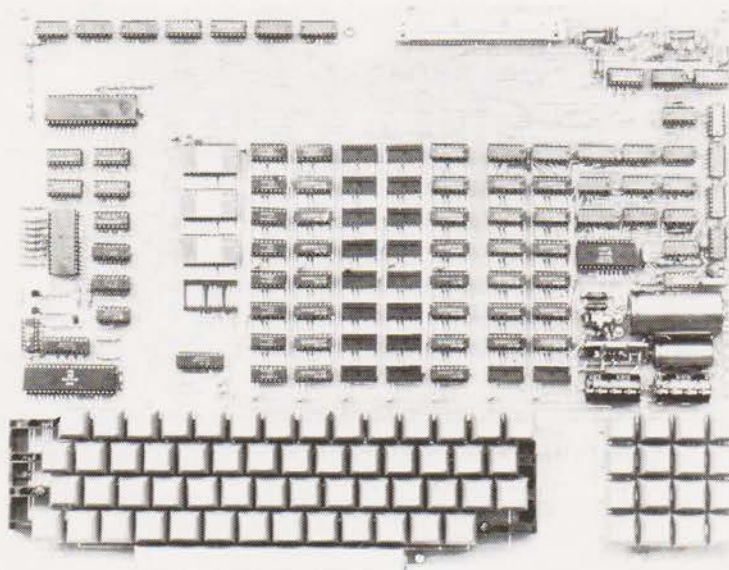
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VOL. 1, NO. 6
AUG. 1979

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	PAGE
NEWS	5
All that goes on goes in!	
ACORN REVIEW	13
When it's small it's how it's used. . . how good can ACORN be?	
GRAVE WORK FOR PET	22
Dead good application report!	
SOFTSPOT	61
Entertaining routines!	
NANOCOMPUTER	31
Micro training system	
PET BUS EXPLAINED	37
Just the ticket	
MOTOROLA PIAs	41
Putting it in and getting it out again in one piece	
5000 AD	54
Eat yer mask off Darth Vader	
PRINTOUT	28
All your own words	
NASCOM TELE-TEST	64
Be spotty on screen	
TRS-80 MINI LEDGER	70
Account for this.	

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Distributed by Argus Distribution Ltd. Printed by LSG. Limited, Lincoln.

EDITORIAL AND ADVERTISEMENT OFFICE
145 Charing Cross Road, London WC2H 0EE. Telephone 01-437 1002/3/4/5

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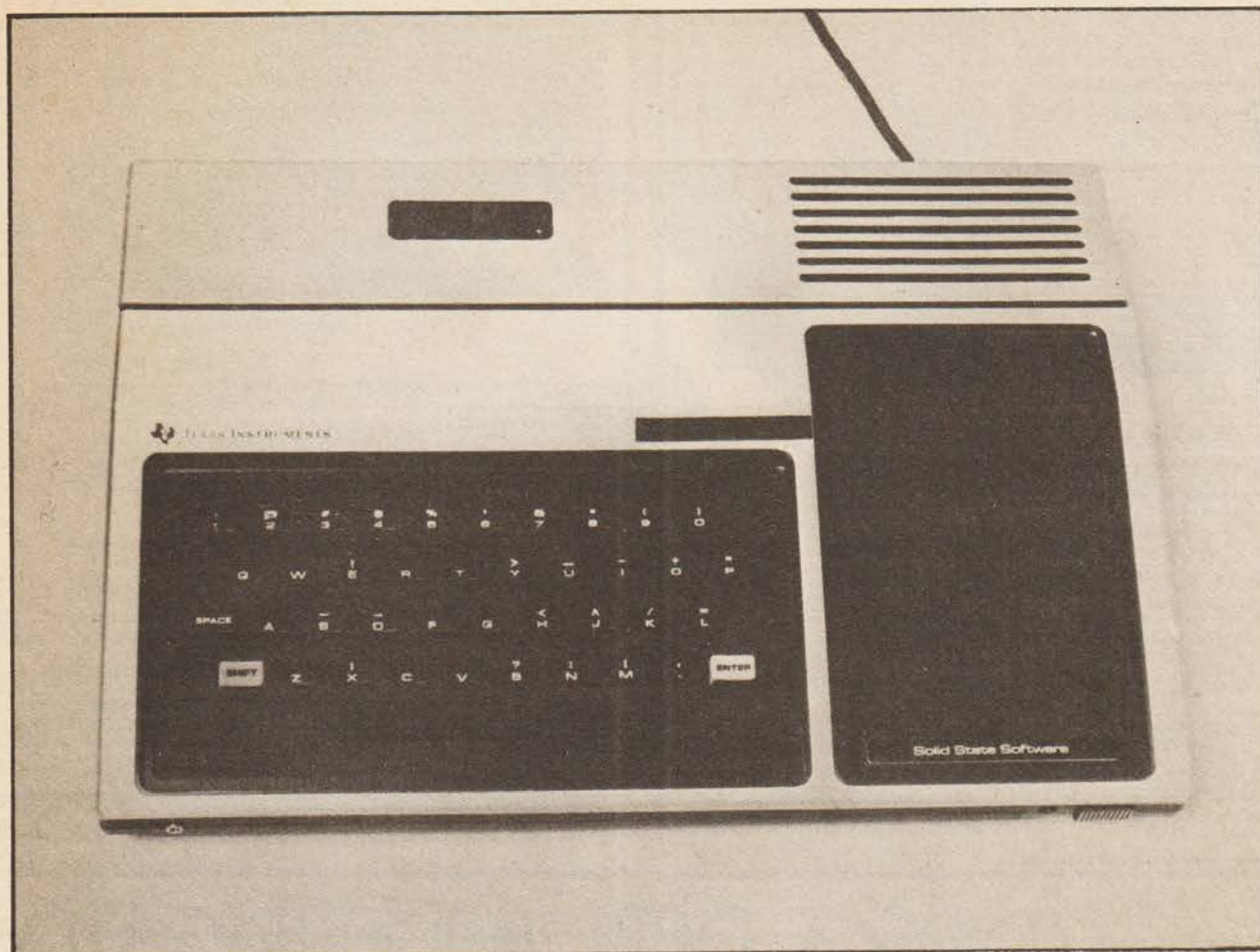
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TRADE ENQUIRIES WELCOME



TEXAS REVEALED

Because the news item on the Texas home computer in last month's issue was rather a stop press affair we had to hold the photo back. Here it is in all its glory and a little more information. The machine is based on the TM9900 16 bit processor, as expected, and the comment from the rest of the industry generally seems to be one of relief rather than worry. The machine even rated a mention in the Sunday Telegraph, the height of respectability?

HARDING RENAMES

The TRS-80 software house of A.J. Harding is now known as A.J. Harding (Molimerx). Molimerx is a loose Latin translation of software, believe it or not! New software available includes a Level III BASIC from Microsoft, Newdos which will replace TRS DOS 2.1, a game called Corplan and a games series called Adventure. All these are up to the usual high standard and for further details please contact A.J. Harding (Molimerx) at 28 Collington Avenue, Bexhill on sea, E.Sussex or ring 0424-220391.

NASCOM NEWS

At last we have had a newsletter from the INMC. Numbered as issue 2, we never saw No.1, it contains a variety of hardware and software notes, as well as some programs. The address to write to for club details is INMC, c/o Nascom Microcomputers Ltd, 121 High Street, Berkhamsted, Herts HP4 2DJ. Also in the news this month is

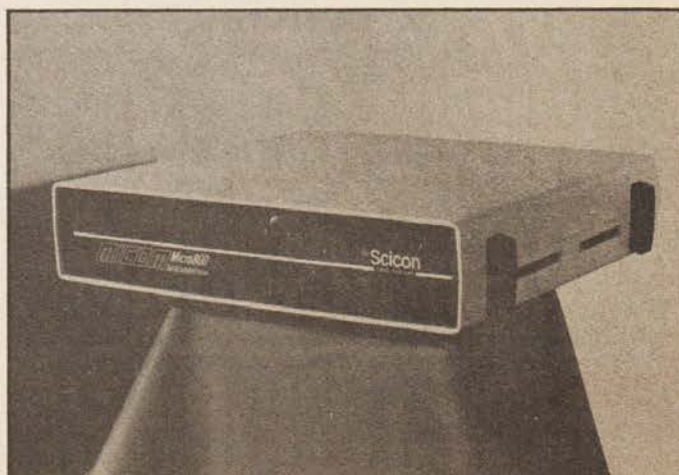
ex Nascom Software Director, Tony Rundle who has left to form a software company called Starbase. They will be producing software initially for Nascom 1 and 2 but hope to expand to PET and Superboard. Users with proven software are invited to submit for publication under royalty. Contact Starbase on St Albans 33137 or write to Waxhouse Gate, 15 High Street, St Albans, Herts AL3 4EH.

CROMENCO DEAL AGAIN

Sheffield is the latest target for Cromenco, they have just appointed Datron as dealers for their range. Typical system prices are £6250 for the Z2-H and system 3 at £3444. Datron also supply the ITT 2020 and a range of software, peripherals and books. Datron are to be found at 1 Prospect Place, Sheffield S17 4HZ.

STATISTICS SELL

Scion Computer Services have installed 100 Micom Micro 800 statistical multiplexers in 6 months. Micro controlled it allows up to 16 asynchronous data terminals to share a single line and up to two synchronous devices at the same time. Options are available for speeds between 50 and 9600 Band and all have built in test facilities. By using statistical techniques the unit can double the channel capacity of a conventional time division multiplexer by assigning data rates dynamically. For more information write to Scion at Brick Close, Kiln Farm, Milton Keynes MK11 3EJ or ring 0908-505656.



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Send large SAE for full catalogue and price list.



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ANALYSE YOUR PROBLEMS

Motorola have brought out a new microcomputer analyser designated the M68 UCANA, try saying that quickly! Designed as a stand-alone portable test unit it can be used for checking out 6800 based systems. Weighing in at 21 pounds and fitted into an attache case it would be ideal for a field engineer. The unit provides both in circuit circulation and signature analysis allowing tests to be carried out at both system and component levels. For more detail contact Motorola at York House, Empire Way, Wembley, Middx HA9 0PR.

NEWBEAR CUT COST

Prices of both the SYM-1 and KTM-2 have been reduced by Newbear. The SYM single board computer based on the 6502 with keypad, 4K monitor in ROM and 1K RAM expandable to 4K on board has been reduced to £160 and the 8K BASIC in ROM is available at £75. The KTM-2 keyboard module, useable with SYM-1 or any RS232 serial interface has been reduced to £225. All prices are exclusive of VAT. More details from Newbear at 40 Bartholomew Street, Newbury RG11 5LL or ring 0635-30505.

RED IS THE COLOUR

Our apologies are due to Trans-Am who loaned us the Compu-color for review in our June issue. We neglected to credit them for their assistance in the production of the article, sorry chaps.

FULL FLOPPY FOR TRS-80

Parasitic Engineering of Berkley, California have announced a full sized floppy for Tandy's TRS-80. Based on the Shugart 800 it is fully compatible with existing units and can be inter-mixed. Plugging directly into the expansion interface it converts the controller from 5¼" to 8" and/or 5¼" and allows continued expansion via the port. Selling for \$995 inclusive you should contact Parasitic at Box 6314, Albany, CA94706 for details.

ITS LOGICAL!

Vero have produced a new double Eurocard for their VIP's range. Totally uncommitted it is fitted with gold plated terminals, two 96 by 96 indirect miniwrap connectors and is designed for wire wrapping prototypes. The board can carry 8 to 60 pin IC's and has both ground and power rails. For more info please write to Vero Electronics at the Industrial Estate, Chandlers Ford, Eastleigh, Hampshire SO5 3ZR.

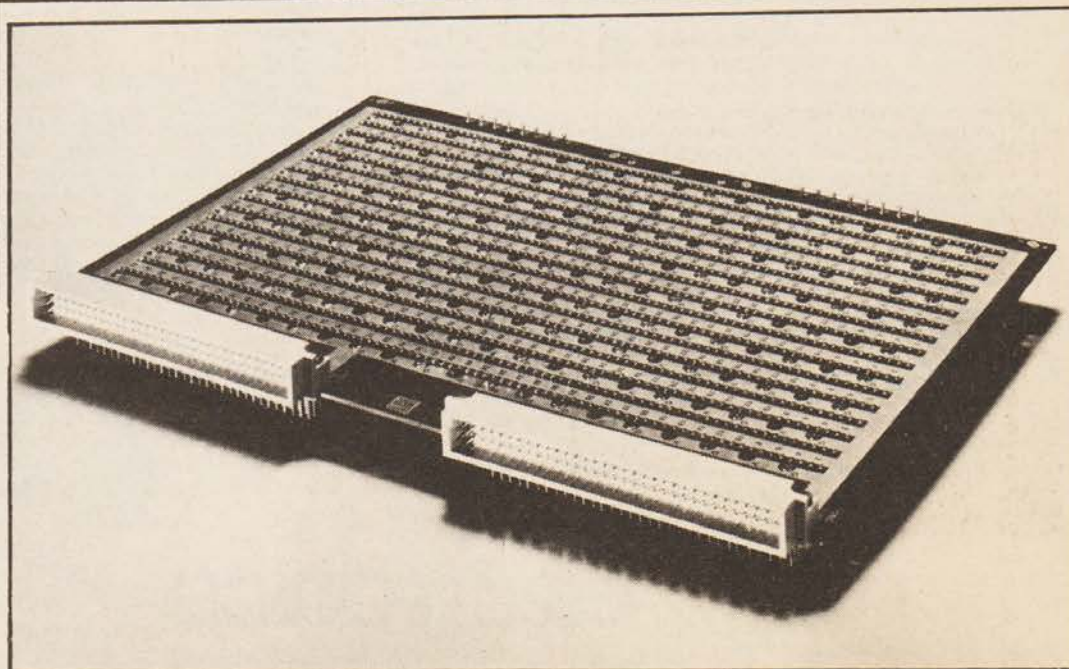
NASCOM HARDWARE

Exclusively announced to us this week was news of an analogue output control board by Microdigital. Designed to plug directly onto the Nasbus it has sixteen 200 mA relays and can be addressed to any of the 256 ports of the Z80. Access can be made through machine code or BASIC. A bare PCB with manual will cost around £15 but kits will be available. The boards are single sided with gold plated

edge connectors and have the component legends printed on. Designed by Mike Coathup of Microdigital it will use standard low power TTL and will be the first in a range of I/O boards produced for various systems. Next in line is an input board for the Nasbus with 16 channels of analogue information, allowing intelligent real time control of domestic and industrial environments. Contact Microdigital at 25 Brunswick Street, Liverpool L2 0BJ.

GREEN WITH ENVY

Mr. Ian Wallace of Microcomp-uation has rung us to say that contrary to our news on PET business system he has got green screen PET's in stock. You'll find him at 8 Station Parade, Southgate, London N14, or ring 01-882 5104.



Happy Memories

21L02 450 ns 83p 2114 450 ns £5.27 4116 300 ns £7.93
21L02 250 ns £1.01 2114 250 ns £5.75 2708 450 ns £7.72

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Low Profile)	Pins:	8	14	16	18	20	22	24	28	40
DIL Sockets)	Pence:	11	12	13	18	19	21	23	30	40

Our new shop is now open at the address below. We shall be stocking a wide range of items to interest all those of you who are building or plan to build your own micro computer, why not pay us a visit? We are open from Mon to Sat 10 to 6 and often much later.

We stock a range of books covering fundamentals through to advanced topics (Like games)

We are NASCOM dealers for the South Coast.

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Our stocks are rapidly increasing; please write or call for latest lists of available products. We welcome your suggestions for stock lines. What do you find difficult to obtain? (We know about buffers)

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has landed* **£499**
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The U.K.-designed and manufactured Novapak disk system for Commodore's PET*, first seen at Compec '78, is (after extensive industrial evaluation), now available to the domestic user. Its unique saddle configuration continues the integrated design concept of your PET, with no trailing wires or bulky desk-top modules.

*Novapak may be used with any available RAM plane.

*May be used with latest versions of PET.

*Data transfer takes place at 15,000 char/sec — effectively 1,000 times faster than cassette!

*Storage capacity is 125 K/bytes (unformatted) on 40 tracks per diskette side.

*Dual index sensors permit dual-side recording for 250 K/bytes per diskette.

*Easy operation full-width doors prevent media damage.

*System expandable to ½ Mbyte on-line storage (4 drives).

*Dual head and 2D versions provide 2 Mbytes on-line.

*Industry Standard IBM 3740 recording format for industry-wide media compatibility offered only by NOVA-PAK.

*Dedicated Intel 8048 microprocessor and 1771 FDC minimise PET software overhead.

*Local hardware and software support available, including applications, packages for small business use.

The sophisticated Disk Operating System is disk-resident, which allows for future DOS-enhancements without hardware alterations. PDOS supports multiple file handling, allocating disk space dynamically to each as and when necessary. Any file may occupy from 1 to 600 sectors as required, at up to 16 non-contiguous locations on the disk. PDOS may be used alone, or within a BASIC program and offers user-specified password security for any file. Multiple access-modes simplify BASIC program construction, and the user may generate tailored DOS modules.

Novapak dual-disk system complete with PDOS and BASIC demonstration programs on disc **£899 + VAT**.

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MEGA BUBBLES ARE HERE

Intel have launched a 1 MB bubble memory with a supporting cast of chips. Called the 7110 it is organised as a serial in, parallel loop, serial out register and holds 2048 by 512-bit pages. Each page is processed as 64 eight bit bytes. Average access time is estimated at 40 mS, maximum is twice the shift rate or 100 kHz. The chip actually holds spare loops, and by using the 7242 formatting chip to decode makes any unused loops transparent to the user. For further details on this solid state marvel contact Intel on Oxford (0865) 771431 or write to 4 Between Towns Road, Cowley, Oxford OX4 3NB.

PET BOOK

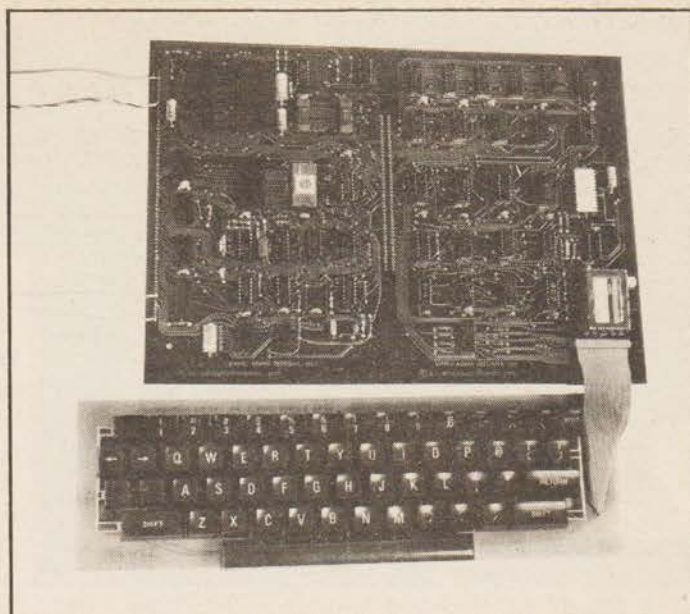
Two lecturers from the University of Ulster have produced a booklet on the PET. Mainly aimed at improving the usage of the machine it deals only incidentally with programming. The book covers such subjects as PEEK and POKE, Tape Management and Presentation and has a set of useful tables for screen and keyboard locations at the back. For your copy of this read only floppy send £1 to Seamus Dunn and Valerie Morgan, The Education Centre, The New University of Ulster, Coleraine, N.Ireland.

EXHIBITION NEWS

Ed Tech '79 will feature several microcomputer systems. Among the exhibitors linked up are Commodore, Research Machines, Digico, Kendata Peripherals, Compelec and many more. There will be a half day seminar on Mini-computers in Education, fee £15, but the show will be free. Dates are 21st to 23rd August at Holland Park School, Airlie Gardens, London W8 and for more information and free tickets please contact The Organiser, Ed Tech '79, Stereoscopic Television Ltd, 41-43 Charlbert Street, St Johns Wood London NW8 6JN.

PET SOFTWARE

Supersoft are producing software for the Commodore PET. Their latest catalogue contains a wide variety of programs including Renumbr, Supersave, Assembler MK1 and 2, Delete and Reverse. A range of business, mathematical and games programs are also available. Among the games are Nim, Bulls and Cows (the original mastermind) a heuristic (learning) version of Stone Paper Scissors, Surround and Sweeper. Also available are C12 cassettes at £3.95 for 10. Software prices range from £1.49 to £9.99 and more information is available from Supersoft at 28 Burwood Avenue, Eastcote, Pinner, Middlesex or phone 01-866 3326.



DUAL CPU EVALUATION KIT

A new processor evaluation kit, with a difference, has been launched by B.L. Microelectronics Ltd. Configured on a Double-double Eurocard PCB it features the option of evaluating the Z80 eight bit CPU or the TMS 9980 sixteen bit CPU. Each processor has its monitor and line by line micro-assembler supplied in EPROM and there is a keyboard and TV interface. The board may be cut in half to give a processor card with choice of CPU and the keyboard/TV card. 1K of RAM is available for the user and up to 4K of 2716 or 2708 EPROM may be accommodated. A 300 Band cassette interface is also supplied using a modified Kansas City standard, and an optional RS232 port is available. Prices range from £194 for Z80 only to £225 for both CPU's and further details can be obtained from B.L. Microelectronics at 1 Willow Way, Loudwater, Bucks HP11 1JR.

DATA TYPE, DATA TERM

A new terminal has been produced by Datatype that is micro controlled. Designated the DT2 it has both upper and lower case, separate numeric pad, 24 by 80 display and an addressable cursor. Baud rates are selectable from 75 to 19200 and optional extras include a buffered printer port, second page of memory and a video output. The device is expected to dent the dumb terminal market and will be supported by Data Type Terminals of Ouit 73, Springvale Industrial Estate, Greenforge Way, Cwmbran, Gwent, Wales.

CLUB NEWS

A varied bunch this month while we await your reaction to our club survey in July. Please keep the information coming in, it will generally be printed in ETI microfile as well to increase coverage.

For those in the Nottingham area into Nascom a new club is being set up by Mr. K.S. Swainson. Meetings will provisionally be monthly and it is hoped to provide a newsletter and a program exchange service. No fees have been set yet. For details write to Mr. Swainson at 9 Brayton Crescent, Highbury Vale Estate, Bulwell, Nottingham NG6 9DZ.

A TRS 80 program exchange is being planned by Chris Cain. He has facilities to test software and copy it under any TRS 80 format. Anyone interested in helping to run or supplying programs for this venture should contact Chris at Eng. Wing, RAF West Drayton, Middlesex.

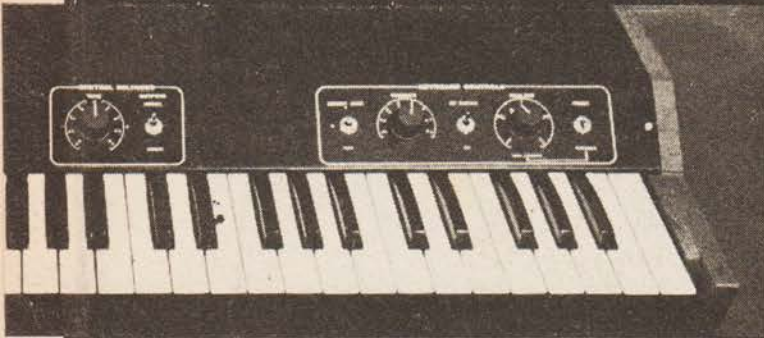
An Exidy Users Group has been set up by Micro44 of Woking. Supplying a monthly newsletter with material from both the US and UK users the membership is set at £5 a year. For membership information contact Andy Marshall at Micro44, 44 Arthurs Bridge Road, Woking GU21 4NT or ring 04862-66084.

And finally this month a plea from one of our younger readers. If anyone is interested in forming a Young Peoples User Group would they please contact N. Sutcliffe Esq. at 1 Suncliffe Road, Higher Reedley, Nr Burnley, Lancashire BB9 5EP with details of your interest. Please enclose an SAE.



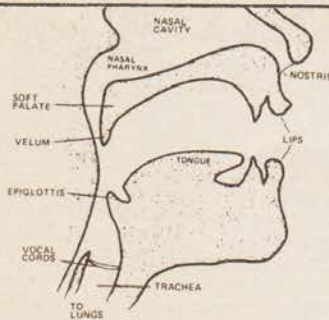
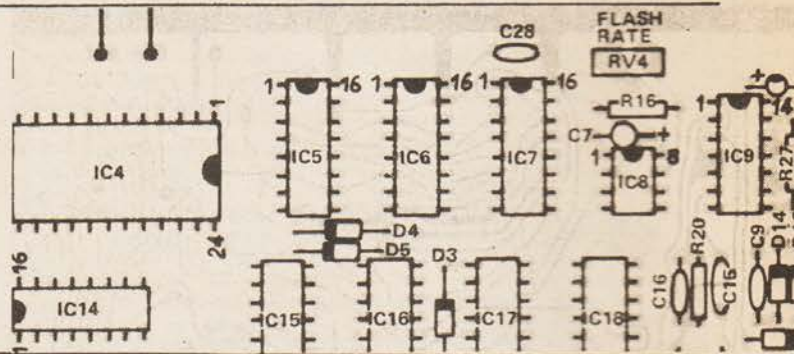
computing today

WHAT TO LOOK FOR
IN THE SEPTEMBER ISSUE
ON SALE AUGUST 24th.



We have featured music making computers before but this month we show you how to connect a micro to the Arak VIII, ETI's Polyphonic Keyboard Controller. Written by Tony Keane, the designer, it should strike the right note with K9.

Our project this month is a BCD to Hex converter that allows you to solve your micro programming problems. Built on a single board it will allow you to key in your binary instructions and get back the Hex code.



Since HAL of "2001" fame brought speech recognition to popular fame many people have wondered how it can be done. Our intrepid reporter investigates the current state of the art and we are sure that you will be suprised.

Our Softspot feature is very popular and this month we offer a program called "Brands". It will have you racing round your TV for hours.

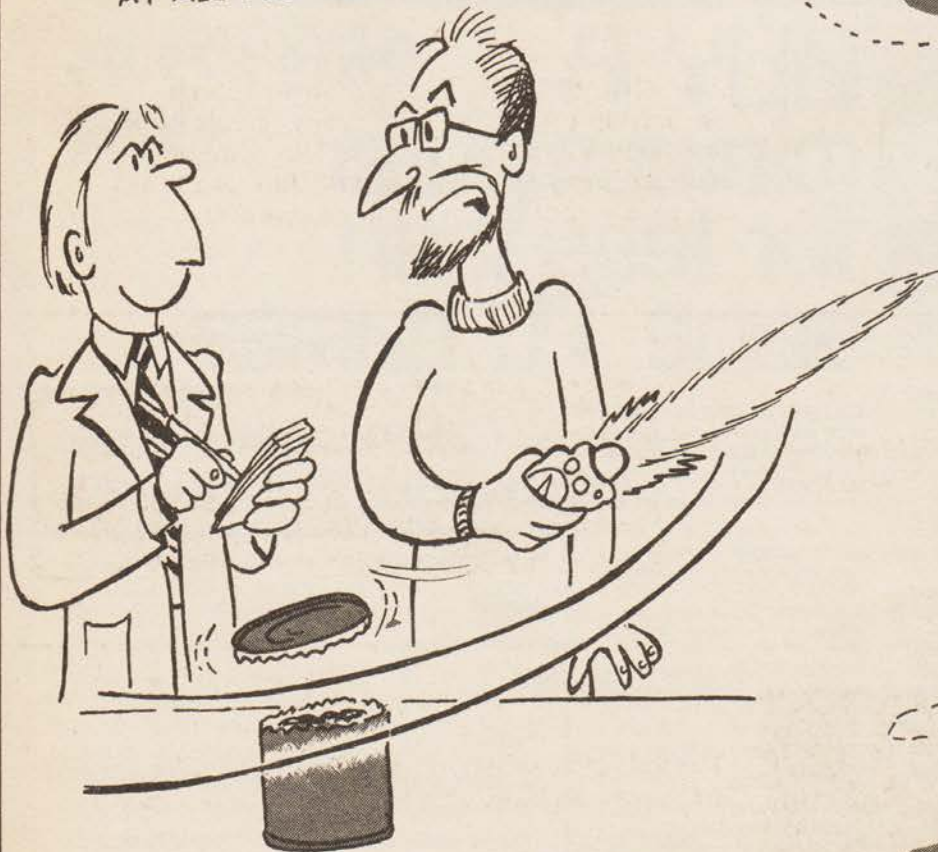
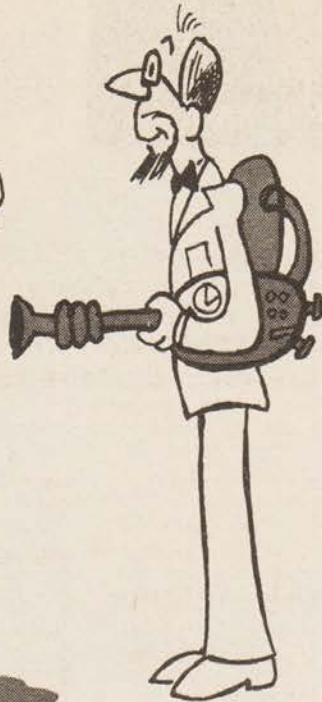


The exhibition scene always hots up in Summer and we report on three very varied ones in our next issue.

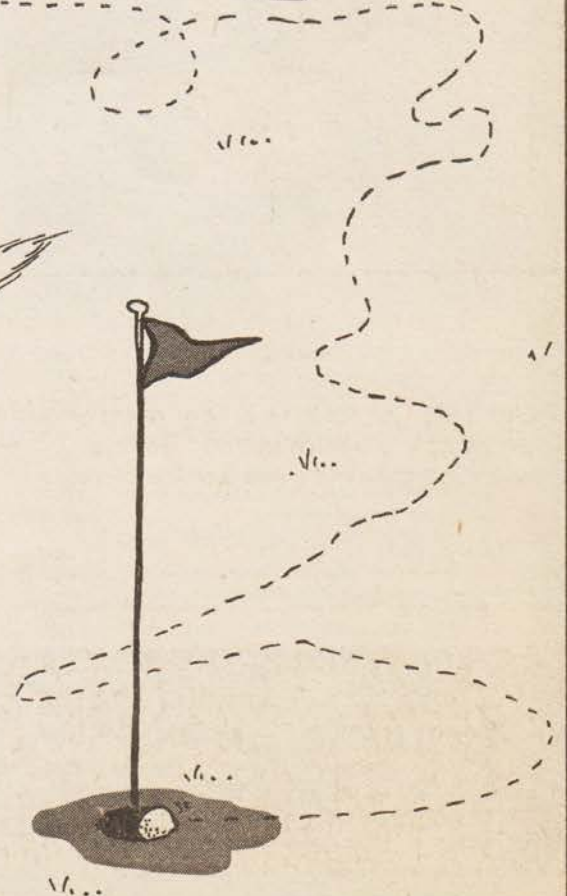




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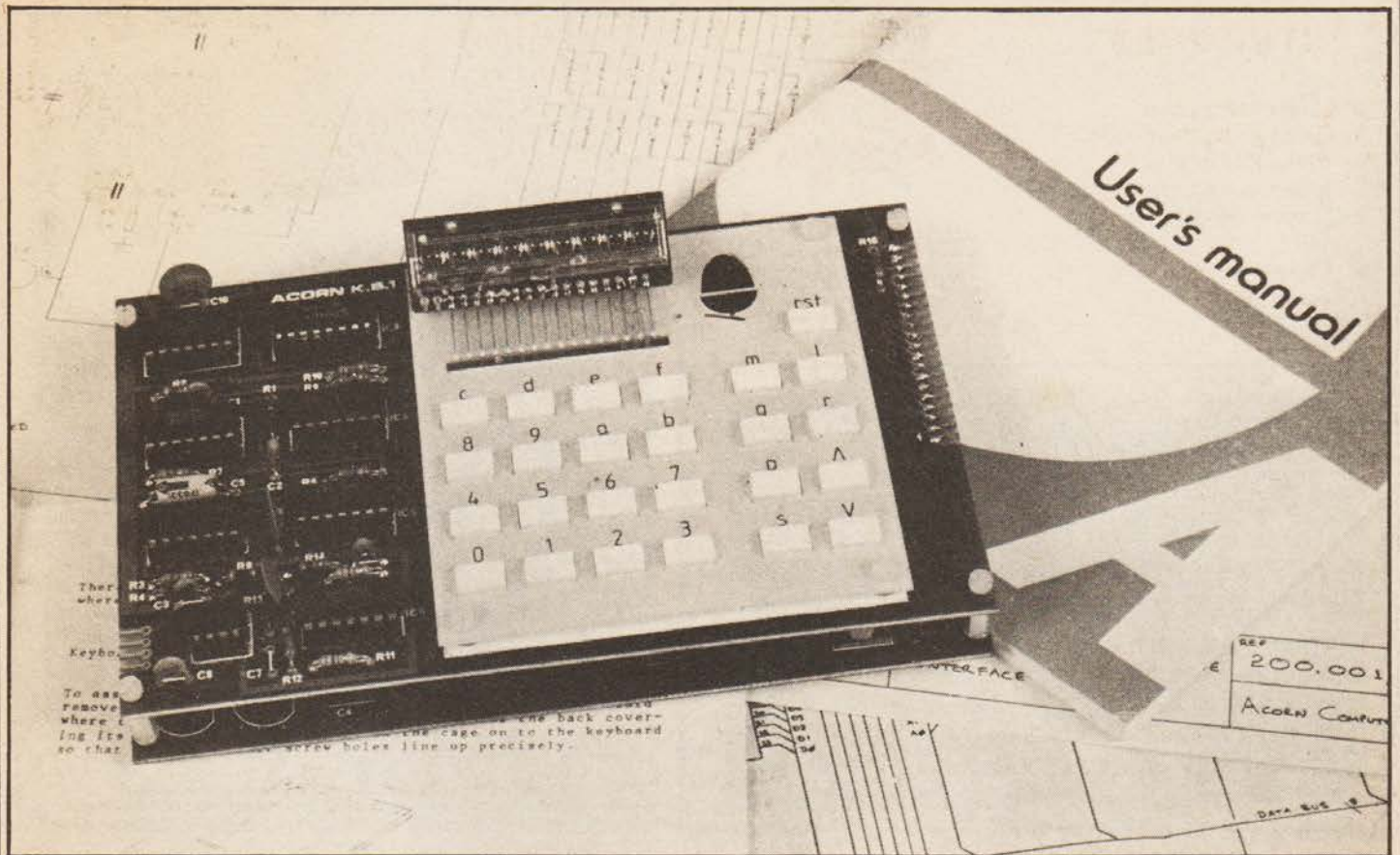
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ACORN REVIEW



A rival for MK14?

One of the most common starting points to home computing often seems to be with a simple kit such as the MK14 from Science of Cambridge. Using the very popular and possibly rather "old-fashioned" SCMP micro it is a very good way to become involved, indeed we are basing our Microprocessors By Experiment series around it. The second most popular micro around seems to be the 6502, as used in the PET, KIM and Apple home computers. A new company called Acorn Computers have now produced a kit based on this chip called Acorn and we decided to take a look at what it had to offer.

What The Postman Brought

The complete kit which we obtained consisted of two PCB's, a bag full of components and a piece of anti-static foam full of ICs and sockets. Also included were circuit diagrams, the constructional manual and the instructions.

We carefully checked out the components to see if we had all that we were supposed to, the header for address selection was missing but everything else was there. No real problem, we 'borrowed' one from the workshops and got down to building it. Using a fine tipped soldering iron is a must with the fine tracks on the boards but we had no real problems as the boards are of very high quality, double sided, plated thru' and solder masked to prevent blobs or whiskers. The only worry we had was in the component identification, the resistor colour codes looked remarkably alike in some cases but the trusty Avo soon solved that. The main gripe was with the capacitors whose codes were unlike any in the manual, good detective work soon proved that 101 meant

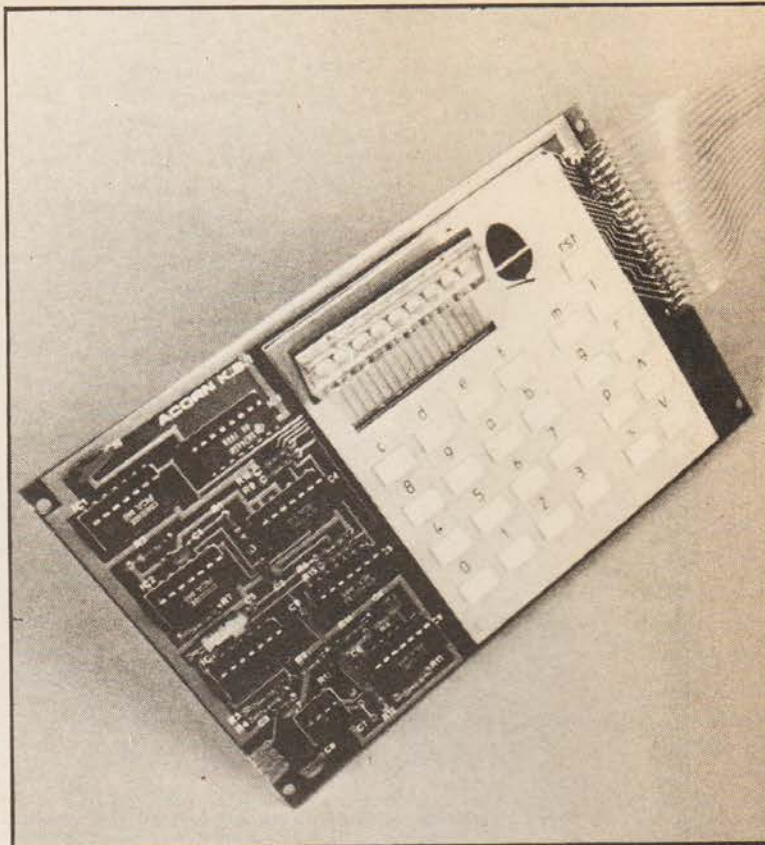
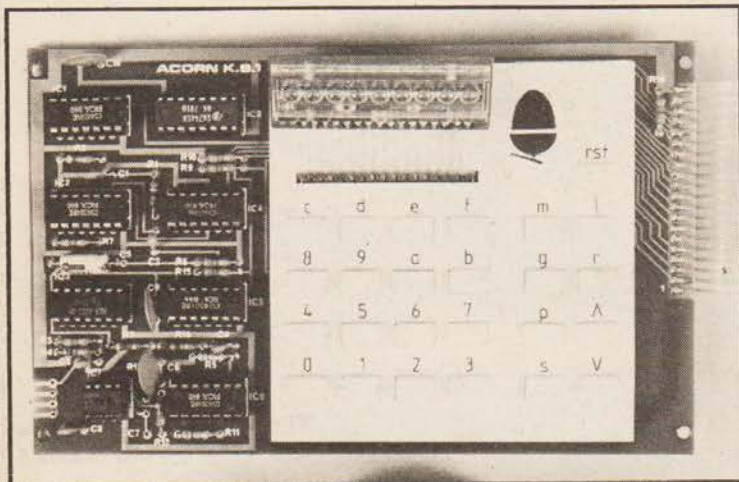
100 pF, 102 was 1 nF and 103 was 10 nF, simple really if you know the answer! However these minor problems do not detract from the fact that the board labelling is good, and provided you can solder competently you should have no trouble at all in building it. One recommendation which will save frayed tempers is to solder the short length of Spectra Strip into the board and then build the keyboard over the top, rather than the way suggested in the manual, it is very fiddly otherwise. A word of caution is also in order about the keyboard, it looks very daunting to build but in reality it only takes a couple of minutes if you go slowly and by the book, don't try short cuts because once it has been built it will be very hard to take apart.

We took about four hours to build the kit, but time is not important as provided you end up with a working kit you'll be happy! Ours worked first time and still does even after much taking apart and putting back for photography and demonstration.

Manual Application

The manual supplied with the Acorn is fairly thorough in its presentation of the necessary information but sometimes it is a little confused. However if you carefully read each section and try out all the experimental programs you should have no problems. As well as covering the 6502 programming the manual goes into binary arithmetic in quite reasonable detail and also covers the hardware of the kit. The hardware section deals with the CPU and general hardware structure of the kit in reasonable detail, it also includes one or two tips on modifications for single step and changing memory types.

Full details of the ASCII codes for display on seven segments are given in the appendices along with the 6502 instruction set, a Hex to Decimal conversion table and the



monitor address information. It would be helpful to have the 6502 manual as well for more detailed information but the book covers all you need to know to begin with.

There are a selection of useful programs supplied as well, varying from games to mathematical routines and all the ones that we tried appeared to work well.

Monitoring The Situation

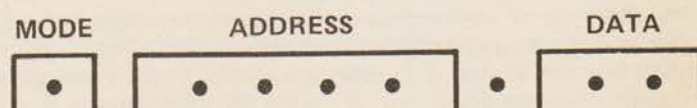
Acorn's built in monitor occupies two 516 by 4 PROMS, coded blue for the high nibble and yellow for low nibble.

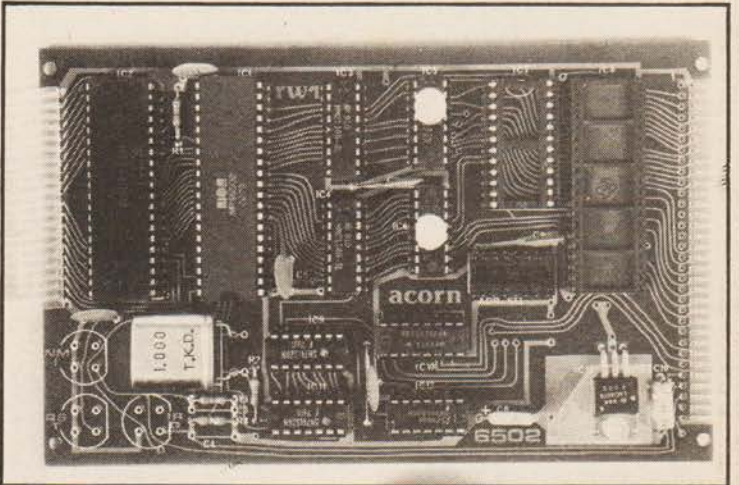
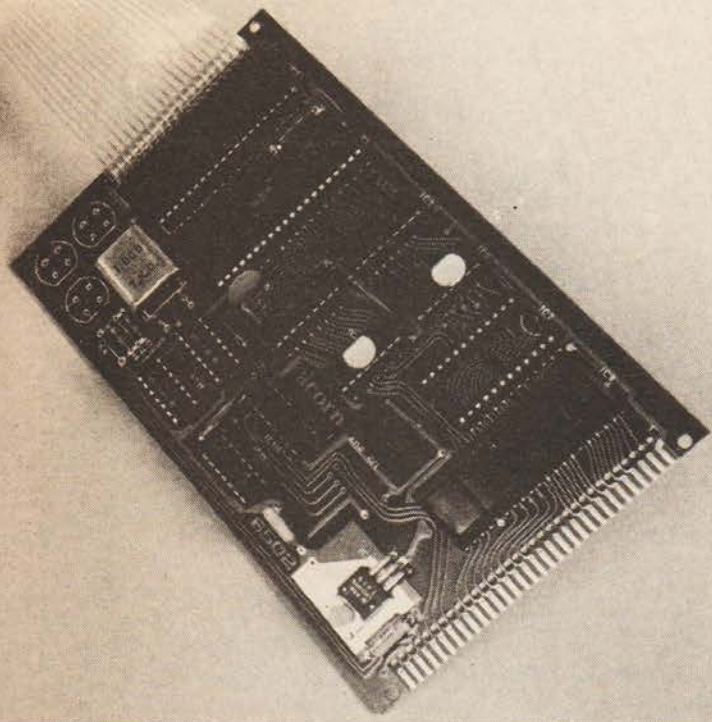
The address range is set by the DIP header socket but they will normally be used in the range F800 to FFFF. The first available commands are M, ^, V. M enters the memory modify mode, allowing you to choose any address in the selected memory area. The letter A appears in the mode display to show that you are in Alter Mode. Pressing any of the eight command keys will display the contents of this address on the right hand pair of seven segment display, the data pair in Fig 1. Using the ^ and V keys allow you to progress either forwards or backwards through memory inspecting the contents of subsequent addresses.

Modification of the data stored at any address is simply performed by keying in the new data and stepping on with the ^ key. Programs are loaded in this fashion as well. The monitor will also allow you to load programs keyed in for running by use of the G command key. This causes a K to appear in the mode display reminding you that the monitor is waiting for the start address, keying in the correct address and pressing any command key will cause the program to run.

Using these four keys will allow you to load into RAM, check, modify and run any simple program. There are several more available commands that you can use, S, L, P

Fig 1. The display format of the seven segment LED's. All eight dots are lit on RST.





and R. The commands S and L allow you to use the CUTS interface to store and retrieve programs from cassette tape. P allows you to insert break points at any address and will give the processor status at this point, R will reset the processor allowing you to continue.

A complete monitor listing is supplied in the manual, there are some corrections supplied on a separate sheet and you would be well advised to write them into the book.

Expansion Rules OK

Apart from buying the Acorn with its keyboard you can use the processor board as the starting point in your system. Memory expansion is currently available in an 8K by 8K format, that's 8K RAM and 8K PROM on a single Eurocard. Designed to plug onto the bus it is fully buffered and runs off a single 5V rail. The whole system is designed to fit into a Eurocard format 19" rack and a variety of other peripheral cards are in the process of development including a VDU interface and floppy disks.

More software will soon be available, a 4K Editor Assembler Disassembler and a 4K Fast BASIC with disk operating system are both scheduled for release soon.

Comparison with the MK14 is of course fairly inevitable but the Acorn certainly seems to have the edge when it comes to serious expansion capabilities.

Final Comment

In summary the Acorn is well produced and will provide a strong rival to the MK14. The construction of the kit is easy provided you are methodical and competent at soldering and once built you will certainly become familiar with the 6502 machine code. A strong feature of the Acorn is that it has an on-board cassette interface so you will be able to save

programs and also that it is expandable. The memory card is available now, the rest hopefully by the end of the year.

In terms of cost the processor board is very reasonable at £35 and the processor and keyboard together at £65 is not an unreasonable price. We feel it is unlikely that many people will build an Acorn up to a complete system with disks, VDU and printer but as an intelligent controller for home use it certainly has a bright future. We also feel that it may replace the MK14 eventually *but* at the moment with the large market there is certainly room for both.

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Mr. I. Sinclair

Part 2

Continuing our introductory series.....

We now have the world's most basic microprocessor unit set up and ready to go, and we're ready to find out just what a micro can do. Before we start, though, a few reminders on how we refer to different LED's might be useful. Don't worry at this stage about the labels (like NRDS, NADS) which are used to indicate various outputs of the 8060 — we'll explain these as we go along. Throughout this series, we'll use DBS0 to DBS7 to indicate the toggle switches. I've wired the switches so that a toggle up indicates logic 1 — if you've used down for logic 1 you'll have to remember that for yourself! The LED's which indicate data (the ones fixed above the data switches) are referred to as DLED0 to DLED7, to distinguish them from all the other LED's. In this context 0 means the lowest digit of a number, and on the prototype is set at the right hand side of the panel, with 7 (the highest digit) at the left hand side.

Setting It Up

The other two toggle switches are labelled SIN (sounds hopeful!) and reset. The reset switch was wired on the prototype so that toggle down caused the microprocessor to reset, not operating, and the switch had to be up to allow the 8060 to run. In the text, I'll use RESET to mean that the reset switch is active; and CANCEL RESET to indicate that the switch is up, inactive, allowing the 8060 to get on with the job. The use of the push button switch is self-explanatory — the word PUSH indicates when it should be used.

Of the other LED's, the address LED's are referred to by the letters ADDR followed by the pattern. For example, ADDR 0010 means that the third of the address LED's is lit, the others are not. The three status LED's are referred to as FLAG 0, 1, 2 in that order, and the other three LED's by their labels on the 8060; NENOUT, SOUT, and NADS of which explanations follow later. The sooner you can get to know and recognise each LED the quicker you can start on the job of getting to know the 8060.

Making A Slow Start

Before you connect up to the power pack, which must be a 5 V supply (it doesn't have to be stabilised, but stabilisation is preferable, particularly if you're going to use the same supply for other microprocessor work), check the voltage. Make sure that the capacitor marked C* is a 250 uF type, with its +pole connected to line C20. Now connect up to the power supply, and don't forget the earth lead, because several power supply units have isolated + and — connections. Remove any shorting links you've placed across the board between X1 and Y1 or X2 and Y2, and check that there are no other such 'temporary' connections anywhere else, particularly from line A2, since this is one which was earthed to check the action of the latches.

All OK? Switch RESET (toggle down on the prototype, so switching line A7 to earth, and switch power on. You may see a few odd flashes from various LED's and others, in particular, some status LED's may come on. The right hand side LED on the Eurobreadboard, (the one labelled NAD's) will probably glow faintly due to current flowing through its pull-up resistor. Try PUSH, nothing

spectacular should happen. All being well, we're ready to find out a few things about this CPU chip (Central Processing Unit, if you're new to all this). Set all the data switches, DB0 to DB7 to zero. This will be interpreted as a command when it is passed to the microprocessor, because the first group of eight bits (making one byte) which are fed in is always an instruction — we'll see later how the microprocessor separates numbers from instruction codes. The all-zero instruction is the halt instruction, and it's the one which will go at the end of any program.

With the data switches set, CANCEL RESET and watch the LED's on the board. After a few flashes, you find the NENOUT and NADS lit, along with the address 0001. RESET, leave a few seconds, and repeat the CANCEL RESET, but this time watch the LED's DLED 4, DLED 5. They flash briefly before the 8060 comes to a stop with address 0001 showing.

What's happening? The sequence goes something like this. When the reset is cancelled, several clock pulses are used in restoring normal action. When the action starts, the microprocessor first checks the voltage at the pin labelled NENIN — the EN-able IN-put. The N indicates that this is active when set low. Since this terminal is permanently earthed on our board, the microprocessor can go ahead with generating an address. More elaborate systems would use a gated input here, so that the microprocessor could not place a number on the address lines when they were being used by another chip. The other labelled LED is NADS, meaning Address Strobe. This line goes to logic 0 when the microprocessor is putting out information on the data lines, and its use is a particular feature of the 8060. The 8060 uses only 12 address pins, mainly because the applications of the 8060 as a Simple Cost-effective MicroProcessor (hence SC/MP) seldom call for anything like a twelve line address, but just in case of applications which need sixteen lines of address, the 8060 has been organised so that four of the data lines send out address information before they are used for data. This happens when the NADS output is low, so that if you want to detect these additional addresses, you gate the data lines with the NADS pulse. Since only four of the data lines, DB0 to DB3, are used for the extra four address bit, the others are used for 'status' information. When the NADS output is low, DB4 indicates the type of action which will follow — high means an input to the 8060, low an output. DB 5 goes high to indicate that the first byte of an instruction is being fetched, DB 6 indicates a delay (see later) and DB 7 is the halt flag, which comes on when a halt instruction is being carried out — and that's something we'll be looking for.

In our sequence, the, DLED 4 and DLED 5 have flashed to indicate that there is an input to the 8060, and that an instruction is being fetched. The address of this has then been generated by the address register — a counter which has had a pulse routed to it to count to 0001. There is no progress beyond this because of the NHOLD action — the microprocessor stops just at the point when data is to be put into the data pins. At this stage, setting any data switch to 1 will set the corresponding LED to 1.

Leave all the DBS 0 — 7 switches at zero, and keep a

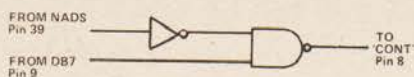
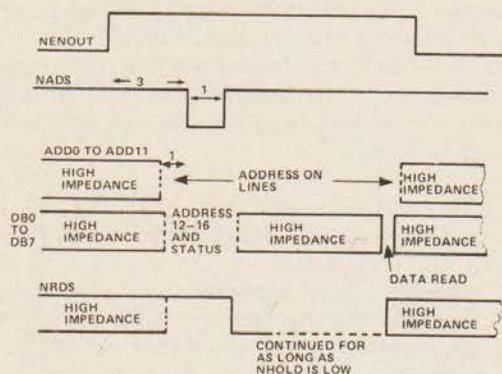


Fig 1. Using gating to ensure that the microprocessor stops on a HALT instruction. This circuitry is not needed for the CHIP-PAN.



NOTE:
DATA IS READ INTO THE 8060 AT THE TRAILING
EDGE OF THE NRDS PULSE.

Fig 2. The sequence of control pulses during a read-data cycle. While NADS is low, the data lines contain four bits of address and also some status signals. The NRDS signal is used for getting the data to the microprocessor to be read, and this data is latched in at the trailing edge of the NRDS signal.

close eye on DLED 7. Press PUSH, momentarily, and you should be rewarded by seeing DLED flash momentarily to indicate that the HALT instruction has been programmed. Now this flash of the DLED 7 lamp occurs just when the NADS pulse is low — it's gated by the same circuit. If we were to arrange a gate so that it is latched to a logic 0 output by the combination of NADS low and DLED 7 high, then this can be connected to cause an automatic halt to a program. The gate output can be connected to the 8060 input marked CONT (continue) on pin 8 (we've connected it to logic 1) so that pin 8 is taken low only when a HALT instruction comes along; this is how a computer using the 8060 would make use of this instruction, but we don't need this facility on our board.

Slow Clocks Generate Problems

Now at this point we can see some disturbing features of microprocessors with slow clock pulses. One odd thing is that the address which is now displayed should be 0010, decimal 2, since the first instruction has been carried out. On my 8060, the address remained at 0001. In addition, you may find various status LED's lighting up, sometimes several seconds after everything else has stopped. You may also find that if the DB 0 — DB 3 switches are changed to 1 while the microprocessor has an address ready and waiting, the address LED's may change also in defiance of all that they are supposed to do. Fear not, and don't claim a refund on your 8060, because all these effects are due to leakage inside the chip. Unlike a board — full of TTL chips, with each input held to logic 0 or 1 by hard wiring and with low resistances, these NMOS chips have appreciable leakage currents between sections. The leakage is very small, but it's enough to flip a bistable over after a few seconds, or even a few hundred milliseconds. When the microprocessor is being clocked at its normal rate of 4MHz or so, this leakage has no effect, because the effect of leakage is cancelled at each clock pulse. With the very slow clock rate we're using, however, these leakage effects can cause odd out-of-sequence flashes. We'll remove these problems later by using a faster clock rate.

Meanwhile, a few more points to note. Point one is that the microprocessor steps take a lot more than one clock pulse to achieve. The data books talk about the number of microcycles per instruction, but you find that there are four clock pulses to a microcycle, so that instructions need upwards of 20 clock pulses to carry out. The brief flash of DLED 7 is around one clock pulse; if you want to compare the clock pulse rate with the time of one cycle, then use an additional LED and 2k7 resistor connected to the clock pulse output on IC4. A suitable connection is C20 — 2k7 to D24; D24 — LED to X2, remembering to connect the LED right way round. With this in place, run through the sequence again, and note how many clock pulses occur between pressing PUSH and stopping at the next address. Note also how many clock pulses are needed after CANCEL RESET before the NENOUT LED indicates the start of an instruction fetch.

The other point is that we have made use of another 'strobe' pulse, labelled NRDS on pin 2 of the 8060. This is the Read Strobe, which goes low when the 8060 is ready to read data (program instructions or numbers) into the data pins. There's another strobe on pin 1, the NWDS (Write strobe) which can be used to indicate when the 8060 is ready

MPU's BY EXPERIMENT

to put data out on the data pins. These strobes are used to avoid any conflict which might arise from using the same data pins both for inputs and outputs, and they are used to activate the devices which send or accept data. In this application we've used only the NRDS strobe to actuate the 74LS126 buffers. With the NRDS strobe high, each input at the 74LS126 is isolated from each output, so that the DB switches have no effect on the DLED output. At the instant when NRDS goes negative, though, the switches connect to the data pins and so also to the LED's. Normally, this strobe pulse is very brief, but when NHOLD is low, the NRDS pulse is extended indefinitely — which is why the DB switches affect the DLED's when the microprocessor is waiting with an address displayed. The NHOLD action also effects the NWDS strobe, though we don't make use of this particular signal, nor do we display it on an LED.

We shall find that it makes its mark however, because when the NWDS strobe is low, the microprocessor is reading out data, and the DLED's can be showing quite a different pattern than is set on the DB switches.

Instructions Diverse

More of that later, though. Let's try another instruction. RESET and wait several seconds. While you're waiting, set the data switches to 10001111, then CANCEL RESET. The usual board LED's will flash up, ending with NENOUT, address 0001 and all the status LED's lit. Now PUSH and leave to settle again. Set to 00000001 and PUSH again. The results you get depend on the leakage in your 8060; on mine, the status lamps started a binary count down, 111,110,101, 011 and so on. If you have endless patience, you can wait and see if it stops. On the other hand, if no status lamps light, you have a low-leakage chip and you may find that everything goes dark for quite a long time. The instruction 10001111 is the delay instruction, and the following figure 00000001 is the amount of the delay. The relation between the second number and the length of delay is rather complicated; Table 1 shows a few examples of the delay as a number of clock pulses from various (low) numbers entered into the 8060.

Now for a grand finale. Reset and wait, meanwhile set up 11000100 on the data switches. Cancel reset, and when address 0001 flashes up, PUSH. Now set the data switches to 11111111 and PUSH again. Now set the data switches to 00000111 and PUSH. This should cause all the status LED's to light and stay on. Depending on leakage, they may light at other times in the cycle, but you will probably find that the status LED's stay lit even when RESET is operated — they will go out only at the next CANCEL RESET.

What this has done is to load the number 11111111 (decimal 255) into the accumulator, which is the main number — handling register. The first byte is the load instruction, the second is the number to be loaded. The third byte is the instruction to copy the number in the accumulator register (store) into the status register — which stores the 1's or 0's, some of which affect the three status LED's.

Next month, we'll speed up the clock rate, and start looking at the effects of instructions, rather than the steps within an instruction.

TABLE 1.

DELAY FUNCTION

When a delay is programmed by using the instruction 10001111 followed by a data byte, the total delay time depends on the clock frequency, the number in the accumulator (Nac) and the value of data (D). If Nac and D are in decimals, then the total delay in clock cycles is given by : $26 + 4(Nac + D) + (1024 \times D)$
For example, if the byte in the accumulator is (decimal) 6 and the data byte is (decimal) 5, then the delay is:

$$26 + 44 + 5120 = 5190 \text{ clock pulses}$$

The time of one clock pulse is given in μs by $1/f$, with f (frequency) in MHz.

A few more examples are shown below. Note that using two bytes to determine the delay makes it possible to program a much larger range of delay than would otherwise be possible.

Data Byte (Decimal)	Delay (clock pulses)
0	26
1	1054
2	2082
3	3110
4	4138
5	5166
6	6194
7	7222

Assuming that the accumulator is set to zero. If the accumulator contains a number, N, then add $4N$ to the numbers shown.

Table 1. Delay functions calculations.

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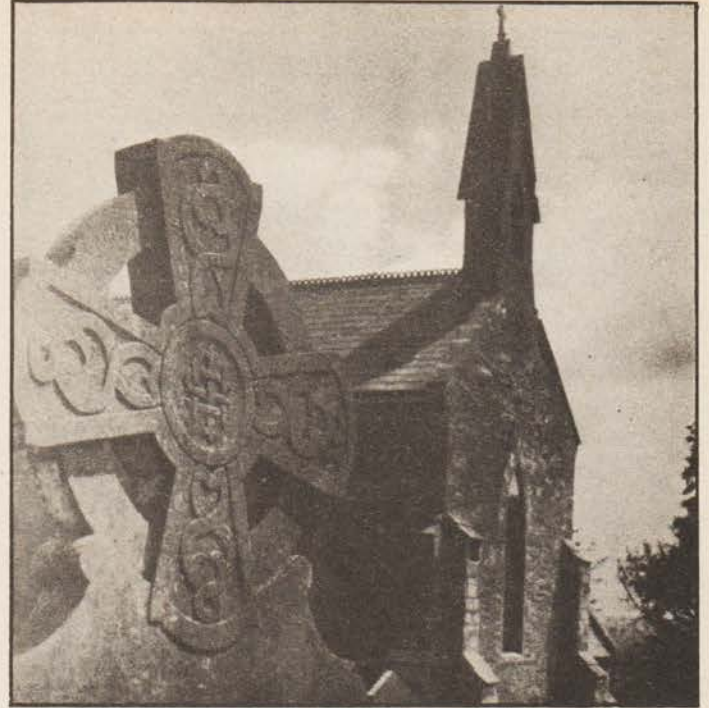
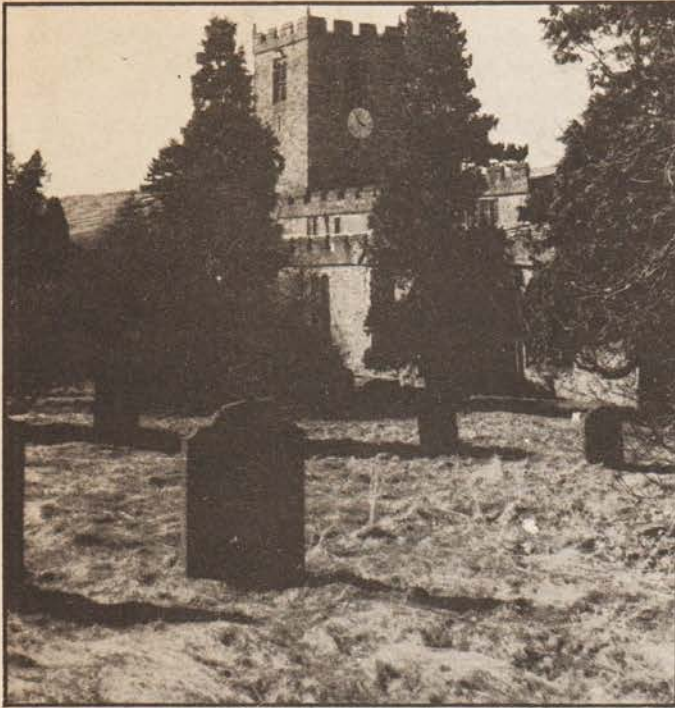
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GRAVE WORK FOR PET



We are always interested in what people are doing with their micros and this application has its roots in history

Storage, handling and interpretation of the large amounts of statistical information such as occurs when reviewing nineteenth century national census returns or analysing eighteenth century Durham coal trade figures can occupy professional historians working in government, university and polytechnic departments, or provide food for thought and enjoyment of amateurs.

For a number of years the professionals have had access to extensive computer facilities when engaged on research work, but until recently few of those dedicated amateurs engaged in local history research have been able to enjoy the availability of such resources. As a result many part-time researchers have spent untold hours collecting, collating and presenting historical data using a range of techniques and equipment which often appear to be as old as the topic under review!

A Revolution

With the introduction of micro-processing technology and computer programming on an increasingly personal scale, the whole range of applied statistical method required by the lone researcher can be revolutionised so that, given the development of a suitable tailor-made programme, much of the tedious time-consuming arithmetic and graphical data-work can be reduced or eliminated.

Parish Register Analysis (Henry VIII And All That)

One important branch of historical research requiring the cooperation of many locally-based investigators, is the

compilation of population statistics from the analysis of 17th century and 18th century parish registers. Such registers were required to be kept in 1538 by order of Henry VIII. As nearly 11,000 parishes were involved, those registers which are complete are of value to historians because they give vital population evidence until 1837 when civil registration became law.

The computer programme described in this article was devised to reduce the tedium of the research exercise requirements covering the marriage, baptism and burial returns for the parish of Grinton situated in remote Swaledale in the north-eastern corner of North Yorkshire. Fortunately for the researchers the Yorkshire Parish Register Society published a modern transcript of the original in one bound volume, thus eliminating subsequent errors of interpreting the varied quality of 18th century handwriting.

The registration period under review was from the year 1700 to 1801, the latter year being important because the first national census took place in 1801, giving the first accurate dating of population size and distribution for the parish area.

The assignment consisted of reviewing the parish register transcript, and from the range of entries compiling separate lists of marriages, baptisms and burials for the 101 years under review. Each year was divided into monthly sections, the return for each month to be recorded to meet the needs of the Cambridge-based Group for the History of Population and Social Structure.

Allowance had to be made for certain sub-classes of event such as entering the number of bastards and sets of twins born each year. On the Burials form there was a column for "Wanderers" which was not used in the exercise as none were indicated in the register.

Because of the strong links between 18th century population control and the state of the nation's internal food supply — a bad harvest followed by a prolonged winter could have an obvious effect on rural parish burial returns during the winter months — all the register monthly totals had to be converted to "Harvest Year" totals so that:—

Burials at Grinton Church in 1779

Decemb^r 22 Hannah Wife of Beeth

8 Eliz^d Wife of John Leates of Tetherham

12 Thomas the son of W^m Spensley of Btades

15 James^r Son of Anth^y Hilditchinson of Btades

25 Eliz^d 4th Daug^r of W^m Spensley of Whitelade by the Parish

28 Ann Dawson of Low Rase By the Parish

January 1780

7 Ann 6th Daug^r of Wm^r Nicholson of Beeth by

9 Joseph 4th Son of John Rase Whitelade of Parish

9 Dorothy 1st Daug^r of Thomas Clarkson of Beeth

12 Joseph Rase near Btades

Register of burials in the parish during parts of the years 1779 and 1780. Family details and place of habitation have all been recorded, making the survey not only one of population but also revealing interfamily relationships.

Burials at Grinton Church in 1780

Feb^r 22 Ann Boates of Grinton by the Parish

March 1 James Bratton of Beeth

20 Peason 2nd Son of Ann Wife of Starkside by the Parish

April 3 The 4th Son of the same Ann of Grinton

13 Abraham Petty of Whitelade

20 Rob^t Carter of Starkside aged 83 years

May 6 Sarah 4th Daug^r of Rich^d Bratton of Beeth

7 Jan^y 4th Wife of W^m Spensley of Whitelade by the Parish

12 Sally 4th Daug^r of Timothy Wind of Btades

24 James 3rd Son of W^m Tom of Btades

27 Nath^l Cowell of Beeth

30 Henry 4th Son of James White of Beeth

30 Ann 4th Wife of James Milner of Beeth

June 3 Christ^{ph} 4th Son of Maryaⁿ Dupson of Beeth

8 Nancy 4th Daug^r of Luke Sutton of Beeth

11 James 4th Daug^r of the same Spensley of Btades

15 Edw^d 4th Son of Edward Smallman of Grinton

17 Ben^t Bell of Beeth

22 W^m 4th Son of W^m Spensley of Whitelade by the Parish

July 26 Sarah 4th Wife of Jan^y Rogers of Hargrave

27 Mary 4th Daug^r of Geo^{rge} Kendal of Grinton

Augst 12 Ann 4th Wife of Grinton by the Parish

18 Thomas 4th Son of John Tansill of Beeth

31 Ann 4th Daug^r of Ralph Smith of Beeth

Oct^{br} 27 George White of Beeth

Nov^{br} 13 The 4th Wife of Beeth

21 John 4th Son of Beeth

(a) For the marriage and burial data the total for the harvest year was obtained by adding the total for August/December of one year, say 1750, to the total for January/July of the next, e.g.

Year	January/July	August/December	Harvest Year Total
1750	35	31	58
1751	27	23	

(b) The calculation of Harvest Year totals differed for the baptism data as the number of conceptions had to be calculated rather than the number of baptisms nine months later. Thus the number of conceptions in the harvest year August 1750 to July 1751 is taken to equal the number of baptisms May 1751 to April 1752.

Year	January/April	May/December	Harvest Year Total
1750	22	25	41
1751	18	21	
1752	20	23	

From the tables of crude totals separate graphs were to be constructed illustrating the annual variation in the number of baptisms, marriages and burials for the research period. In order to reveal parish population trends more clearly and smoothly additional graphs were constructed using the base-time of a nine-year moving average. A natural-increase graph was also drawn from the data obtained by subtracting each annual total of burials from the total of baptisms, another moving-average graph being calculated from this information.

The Pet Problem

This was to obtain a picture of the population in 9-year sliding averages over 101 years prior to the introduction of the National Census. The parish records were consulted for the monthly figures and particulars of baptisms (births), marriages and burials (deaths). Notes were required of evidence of twins, bastard births, out-of-parish marriages, etc.

Part Of The Pet Solution

A PET computer was available and a programme was to be developed having regard for ease of input and with facilities for review, correction, calculation and display of results in both numerical and graphical forms. A data file was established on which all input data would be stored. This was to enable the work to be continued with an 8K memory (RAM) and allow for subsequent use of the stored data.

The program was in three parts, (a) input and amendment, (b) store on data file, and (c) processing of data.

Input And Amendment

The monthly data involved five categories: Male births, Female births (baptisms), Marriages, Male deaths and Female deaths (burials). For each category provision was made for the numerical record 0 - 99 and for two additional characters; a letter if a special event occurred, to be followed by a single digit for the number of such occurrences, e.g. the number of pairs of twins or bastard births.

A quick calculation shows that five categories, each with up to four characters, and a century of twelve months per year, would generate up to 24,000 characters which would exceed the standard PET's memory. The chosen solution

GRAVE WORK FOR PET

ion was to reduce the detailed record to around 2,000 characters by retaining only the annual totals while the data for 12 months of one category would be held and corrected and then passed to a data tape so that the same memory space could be re-used repeatedly and all the corrected entries would be available for subsequent use.

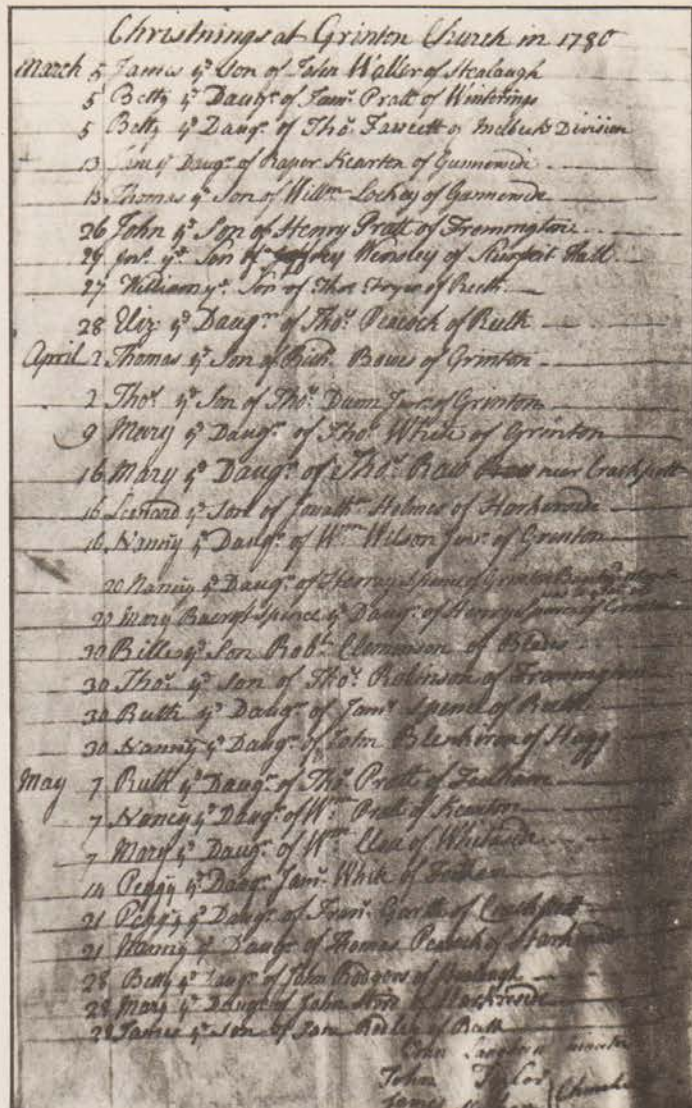
It was also necessary that the keying in of data could be stopped and continued at a later date after PET had been switched off.

Input

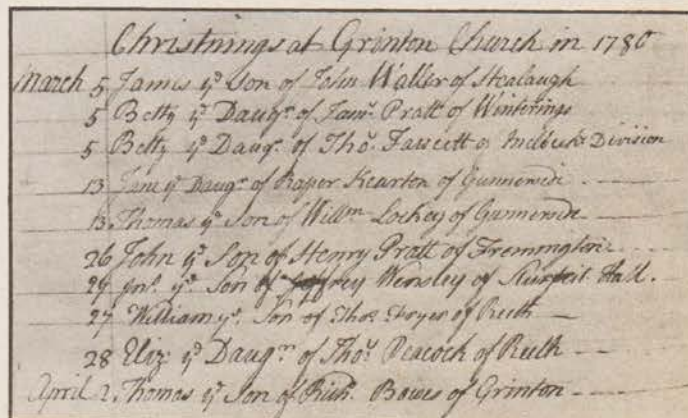
A clear guide was given to the operator at every stage, and allowance for amendment of errors so that each year's entry could be verified and put onto tape before the space in memory which it occupied was used by corresponding entries for the subsequent year.

Consultation between the researcher and the programmer determined the most convenient sequence and method of entry. This was as follows:—

1. State 'start year', 'end year', a maximum of nine 'notes', e.g. P — DIED OF THE PLAGUE, with No.9 being reserved for the general note 'R — REMARK'. (Fig. 1)
2. Data would be read from original parish records, month by month, year by year, until one entry (e.g. male births) was complete and then for the other entries in turn.
3. The operator would enter one digit or two digits (maximum) followed by one of nine letters if there was an associated note, or a Carriage Return. If a letter was entered, the next monthly entry would be accepted only after a number, 0 — 9, associated with the note had been input. (Fig. 2)
4. There was protection so that an incorrect letter could be refused and a letter would not be accepted as the initial character of a monthly entry. There was also protection against the number associated with a note being larger than the monthly entry. E.g. lines 440, 463, 464, 492 and 498.
5. In the case of twins, which was the subject of a note 'T', male twins only would be recorded as the note for male birth entries so that an entry '2T2' might indicate that one pair of twins (both boys) was born that month, or that two pairs of twins (each one boy and one girl) had been recorded; in the latter case there would be a corresponding entry in the female births record.
6. At intervals a group of 12 entries was shown on the screen sequentially, and the operator was asked to confirm or amend each one. (Fig.3) This is a neat and satisfactory system.
7. Provision was made so that the recording of records could be broken off and PET closed down to be reopened for subsequent recording sessions.



Register of christenings that took place in the parish during 1780. The lower picture shows an expanded section for the month of March. The upper register has been signed by the Minister and Church Wardens.



GRAVE WORK FOR PET



Store On Data Files

To conserve memory a data file was opened into which the month's records were entered as the work of reading from parish records proceeded. At the same time annual totals were stored in RAM to be entered on a separate data file held immediately after the programme at the conclusion of each sitting. This latter was overwritten at the end of subsequent sittings, while the data file on which monthly records were retained was in fact a series of consecutive data files on another cassette.

Processing The Data

A second program tape was to be used to read and process the material collected on the data files. Work on this is proceeding but does not present any special problems. One of the big advantages of the whole system is that once the data is on tape it is not necessary to re-enter it if a new theory is to be tested by calculating and displaying different values derived from the original statistics. Thus what was once a time-consuming labour becomes the much more satisfying problem of writing a suitable program of instructions to the ever-patient PET.

Note regarding lines 562 to 599.

The answer to "MORE?" from line 550 will normally be Yes leading to "RETURN" on line 599. The operator has to be very determined to strike N followed by 0 and hence line 5000 which closes the data file and is the action required only at the end of a sitting.

```

30 PRINT"NUMBER OF NOTES (0 - 9)"
40 GETX$:IFX$=" "THEN40
50 N=VAL(X$):DIMNS(N):FORX=1TON
60 PRINT"LETTER ?"
61 GETX$:IFX$=" "THEN61
62 PRINT SPC(9) X$:"":INPUT"NOTL":TS
70 NS(X)=X$+" "+TS:PRINT"NEXT"
400 REM SUB GET 4 CHRS -----
405 PRINT" YEAR "Y+YS-1
410 PRINT"NUMBER OF "ES(E):" IN "MS(M)
415 PRINT" PUT 0-99 FOLLOWED BY":PRINT" RETURN OR LETTER FOR NOTE"
420 FORZ=1TON:PRINTNS(Z):PRINT:NEXTZ
422 PRINT" TO REDO THIS ENTRY PUT "
425 TS=" "
430 IFT$ "THENPRINT"ENTRY = ":TS
432 GOSUB480
435 ONLGOTO440,450,460,490
440 IFA 570RA 480RF=1THENPRINT"REDO 0-99!":GOTO425
445 GOTO430
450 IFX$=" "THEN494
454 IFF=1THENT$=LEFT$(TS,1)+" ":TS(Y)=TS(Y)+TS:RETURN
456 IFA 64ANDA 91THENGOSUB476
458 IFA 64ANDA 91THENT$=TS+" "+X$:GOTO460
459 GOTO430
460 FIX$=" "THEN494
461 IFF=1THENGOSUB476
462 IFF=1THENT$(Y)=TS(Y)+TS+" ":RETURN
463 IFA 65ORA 90THENGOSUB476
464 IFA 65ORA 90THENPRINT"REDO - LETTER OR RETURN":GOTO430
465 FORZ=1TON:1FLEFT$(NS(Z),1)=X$THEN468
466 NEXTZ: GOSUB476
467 PRINT"REDO LETTER OR RETURN":GOTO430
468 PRINT"HOW MANY (0-9) "MID$(NS(Z),5):"?":GOTO430
470 REMSUB-----
476 TS=LEFT$(TS,(L-1)):RETURN
480 F=0:PRINT"?"
482 GETX$:IFX$=CHR$(13)THENF=1
484 IFX$=" "THEN482
486 TS=TS+X$
488 L=LEN(TS):V=VAL(X$):A=ASC(X$)
489 RETURN
490 IFF=1THENGOSUB476
491 IFF=1THENPRINT"REDO":GOTO430
492 IFV VAL(T$) THENPRINT"TOO MANY?-REDO ENTRY":FORZ=1TO2000:NEXT
:GOTO405
493 IFX$ " "THEN495
494 PRINT"OK REDO ENTRY":FORX=1TO1500:NEXT:GOTO405
495 IFA 47ANDA 58THENT$(Y)+TS:PRINTTS:FORZ=1TO20 :NEXT:RETURN
498 PRINT"ONE LETTER ONLY!":GOSUB476
499 GOTO430
500 REM SUB CHECK AND CORRECT -----
508 FORX=1TON:T(X)=0:NEXTX:T=0
510 GOSUB700
511 QS=RIGHT$(TS(Y),48)
513 FORZ=1TO12:X$=MID$(QS,Z*4-3,4)
514 PRINTMS(Z),X$
516 X=VAL(X$):T=T+X
517 FORX=1TON:1FMIDS(X$,3,1)=LEFT$(NS(X),1)THEN:T(X)=T(X)+VAL(RIGHT$(X$,1))
518 NEXTX,2
520 X$=STR$(T)
530 Y$(Y)=Y$(Y)+X$+"*"
531 PRINT"YEAR="Y-1+YS
535 FORX=1TON:PRINT"TOTAL = ":NS(X):" =":T(X)
540 Y$(Y)=Y$(Y)+STR$(T(X))+":":NEXT:PRINT$(Y)
550 PRINT"MORE ?":AS=" "
560 GETX$:IFX$=CHR$(13)THEN560
561 IFX$=" "THEN560
562 IFX$="N"THENPRINTX$:AS=X$:GOTO560
563 IFA$="N"ANDX$="0"THEN5000
599 RETURN
700 REM"---+---+SUBR
705 PRINT"3TS(Y) =":TS(Y)
710 PRINT"NOW EDIT2 AND PRESS RETURN?"
711 FORX=1TO12:X2$=" "
712 X1$=LEFT$(TS(Y),4)
715 PRINT"FOR "MS(X):" - ENTRY IS ":X1$ :PRINT""X1$
721 GETX$:IFX$=CHR$(13)THEN750
722 IFX$=" "THENX2$="":GOTO712
723 IFX$=" "THEN721
724 X2$=X2$+X$:PRINT"1":X2$:1FLEN(X2$) 4 THENX2$=LEFT$(X2$,4):GOTO726
725 GOTO721
726 TS(Y)=RIGHT$(TS(Y),44)+X2$
727 PRINT:PRINT TS(Y):NEXTX

```

The program sections referred to in the text are as follows.

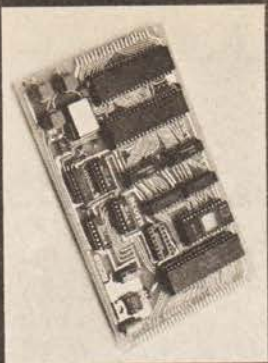
Fig 1 is lines 30 to 70, Fig 2 is lines 400 to 499 and Fig 3 is the final section from 500 to 727.

Acknowledgements

The photographs were taken by L. Cook Esq., and are reproduced by kind permission of the Rev. W.M. Case, Vicar of Grinton with Marrick.

The original parish registers are deposited at the County Records Office, County Hall, Northallerton, North Yorkshire.

Three Trumps from Acorn

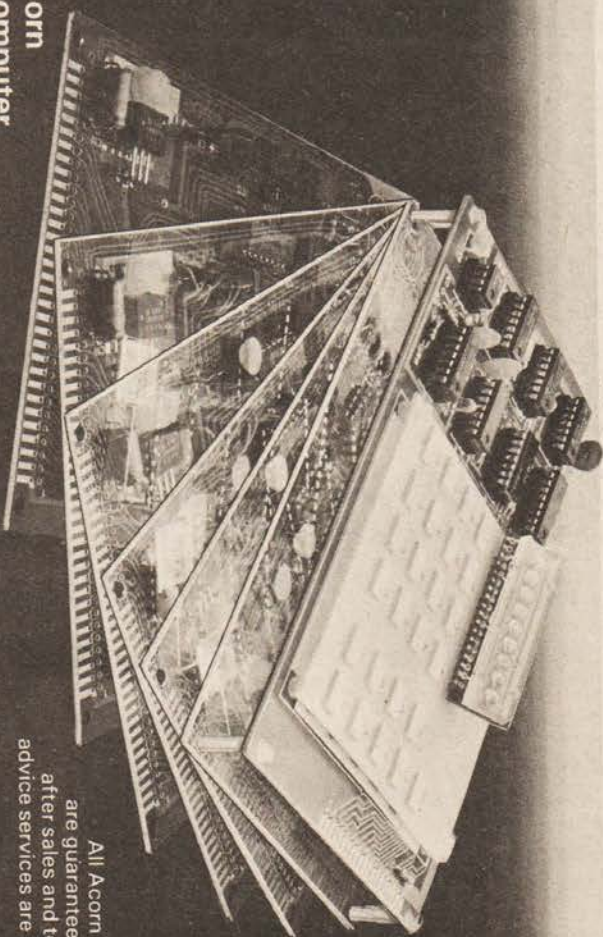


Acorn Controller

Designed as an industrial controller module, it is based on the 6502 CPU with 2K Eprom, 1.25K ram and 32 I/O lines. In eurocard format it is provided with an onboard monitor (2 x 7.45571) giving comprehensive development and debugging facilities. Also available in minimum configuration for low cost OEM applications.

The Acorn Microcomputer

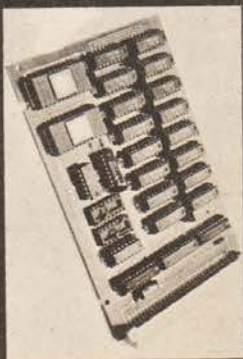
The Acorn controller module mounted beneath a matching eurocard with hex keyboard, 8 digit seven segment display and CUTS tape interface requires only a single unswitched power supply to form the powerful Acorn microcomputer.



All Acorn modules are guaranteed and full after sales and technical advice services are available.

Acorn Memory

The first in our series of expansion cards is the Acorn 8K + 8K 'state of the art' memory module. On a matching eurocard it provides 8K of ram (2114) and 8K of Eprom (2732) or 4K of Eprom (2716). It requires a single 5V rail, is designed for direct connection via a 32 way edge connector to the Acorn bus and is fully buffered for wiring into any system. Two onboard sockets provide independent positioning of Eprom and ram.



Order form

Send to: Acorn Computers Ltd. 4A Market Hill, Cambridge, Cambs.

- ☐ (qty) Acorn Microcomputer(s) in kit form at £65.00 plus £5.20 VAT
 - ☐ (qty) Acorn Microcomputer(s) assembled and tested at £75.00 plus £6.00 VAT
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- N.B. Price shown is for full 8K of ram, prices for smaller memory options and Eprom additions available on request.

I enclose a cheque for £..... made out to Acorn Computers Ltd.

Name _____
Address _____



Regd No
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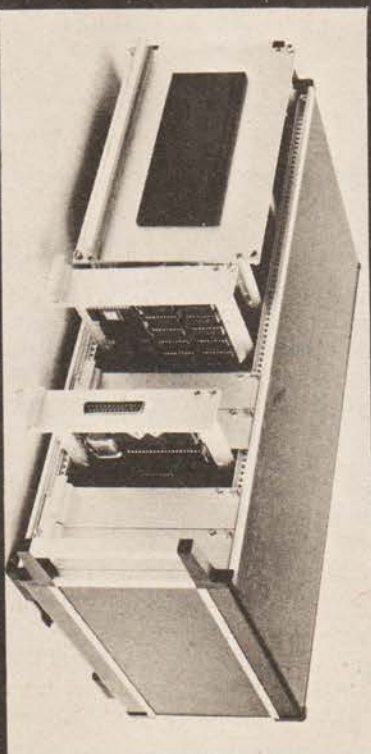
Although designed for expandability the Acorn Microcomputer is a complete development system for the Acorn controller and together with the Acorn Users Manual provides the perfect introduction to hex programming; the carefully optimised monitor has the following functions:

System Program
Set of sub-routines for use in programming
Powerful de-bugging facility displays all internal registers
Tape load and store



Software available soon includes 4K-Editor-Assembler-Disassembler, 4K Proprietary Fast Basic, Disc operating system with full file handling.

Although a standard strip of



veroboard is all that is required for a full backplane, a racking system can be made available by Acorn Computers. The rack shown includes the VDU interface, two memory cards and dual floppy disc interface.

The Editor
Computing Today
25 - 27 Oxford Street,
LONDON W1R 1RF

6th June 1979

Dear Sir,

In response to your recent article on Word Processors and request for details of any other systems, I would like to bring to your notice TEXTIE MK II which was responsible (with the Nascom 1 on which it runs) for the production of this letter. Published by my own Company, The Software Publishing Company, and in its original form designed to support COMPUTA GAZETTE the TEXTIE series of word processors may well have some interesting application for Nascom 1 users.

Uniquely, the documentation for TEXTIE MK II is supplied on the same cassette as the machine code program in such a form that the program description and instructions for use are displayed on the users VDU by the program itself.

It is not pretended that TEXTIE at the present stage is anywhere near a useable commercial package but at 10.00 per cassette the following features are provided:

Printer O/P routine with margin and line length adjust, word wrap-round (i.e. a word that would overlap the margin is used to start the next line)

Buffer accommodates 150 lines which are screen numbered and scrollable

Error checked Tape Read and Write of the whole or any part of the buffer

Typewriter style keyboard and latching shift


Command modes and line numbers continuously displayed

Automatic wrap round on VDU with adjustable line length

Edit commands to open up and swallow space or text

Presently, the program has been demonstrated to amateur user groups at Nottingham, Derby and Liverpool with great interest and it is the intention of my Company to continue product development with a view to producing a very powerful, programmable system.

Yours sincerely,


Frank Butler

8a Church Side,
Mansfield, Notts.

Dear Sir,

As Mr W.M. Davies has criticised some spelling in your paper (which I welcome) perhaps I may ask, through your columns, for one or two other improvements to be made in the computing world's use of our language.

(1) "Data" is a plural word; you cannot talk of "a data" but "a datum". ("Things" or "A thing given".)

(2) Compound words, of which hundreds are generated yearly in the world of technology, demand the use of a hyphen to make two old words into one new one. To take an example at random, from the same page as Mr Davies' letter, a reader writes about a high level language. The language is neither high nor level: it is a high-level language. People tend to be afraid of hyphens because they are not always sure when to use them, so they ban them altogether. The more information accumulates and meanings multiply, the more must our language become: richer, not poorer. Poverty can disguise itself as simplicity. If a meaning is lost or obscured the language is not simple; it is just wrong.

(3) Less important: I turn to the other use of the hyphen; linking the two parts of a word which has to be broken at the end of a word:

(a) The short hyphen is used for this, not the long dash, as seems to be happening throughout your paper. In any case, as your right margin is unjustified on the PRINTOUT page, the words should not be broken.

(b) It matters where you break the word; it should not happen just anywhere. On page 5 (May), in the top paragraph, there is progr - ams. No comment necessary.

(4) One final grouse. We English do not take kindly to innovations, and post codes (used without difficulty in the rest of the literate world) seem to have caused headaches. But how can any computer-minded person not use so obvious a data-processing aid?

Yours sincerely
E.B. Simmons

27 Middleton Road,
Brentwood,
Essex CM15 8DL

Dear Sir,

In your review of the CMC 1200 IEEE to RS232 adapter it is suggested that in order to return the PET to the keyboard mode, a syntax error should be created. The preferred method is to enter PRINT#1 : CLOSE 1. This is essential if it is to be done under program control.

More seriously though, the PET's IEEE - 488 bus is a parallel bus. By plugging in the serial device no other parallel peripheral can be accommodated. This shortfall is commonplace among designers of attachments to the PET, each omitting to provide an IEEE - 488 bus connector to allow further daisy-chaining. How is one supposed to connect the rest of the range of peripherals marketed by the same company, other than one at a time?

Yours sincerely,
R.D. Geere.
(Independent PET Users Group).

52 Highfield Road,
Cove, Farnborough,
Hants GU14 0EB.

Dear Sir,

Thank you for including our Electronic Master Mind in your June issue games review.

I am writing to the magazine to comment on your claim that you have found a method of cheating. By pressing the "Fail" button on the Electronic Master Mind one can indeed release the code flashing its congratulations EXCEPT it doesn't carry with it that magic "Clue" response of 3-0, 4-0 or 5-0.

Remember the eleventh Commandment: "Thou shalt not get found out". I think in this case you would get found out.

Yours faithfully,
Colin Wright.
(Publicity Officer)

INVICTA PLASTICS LIMITED,
Oadby,
Leicester LE2 4LB.

Dear Sir,

Thanking you for your recent letter accepting the article "Appreciating the Microprocessor".

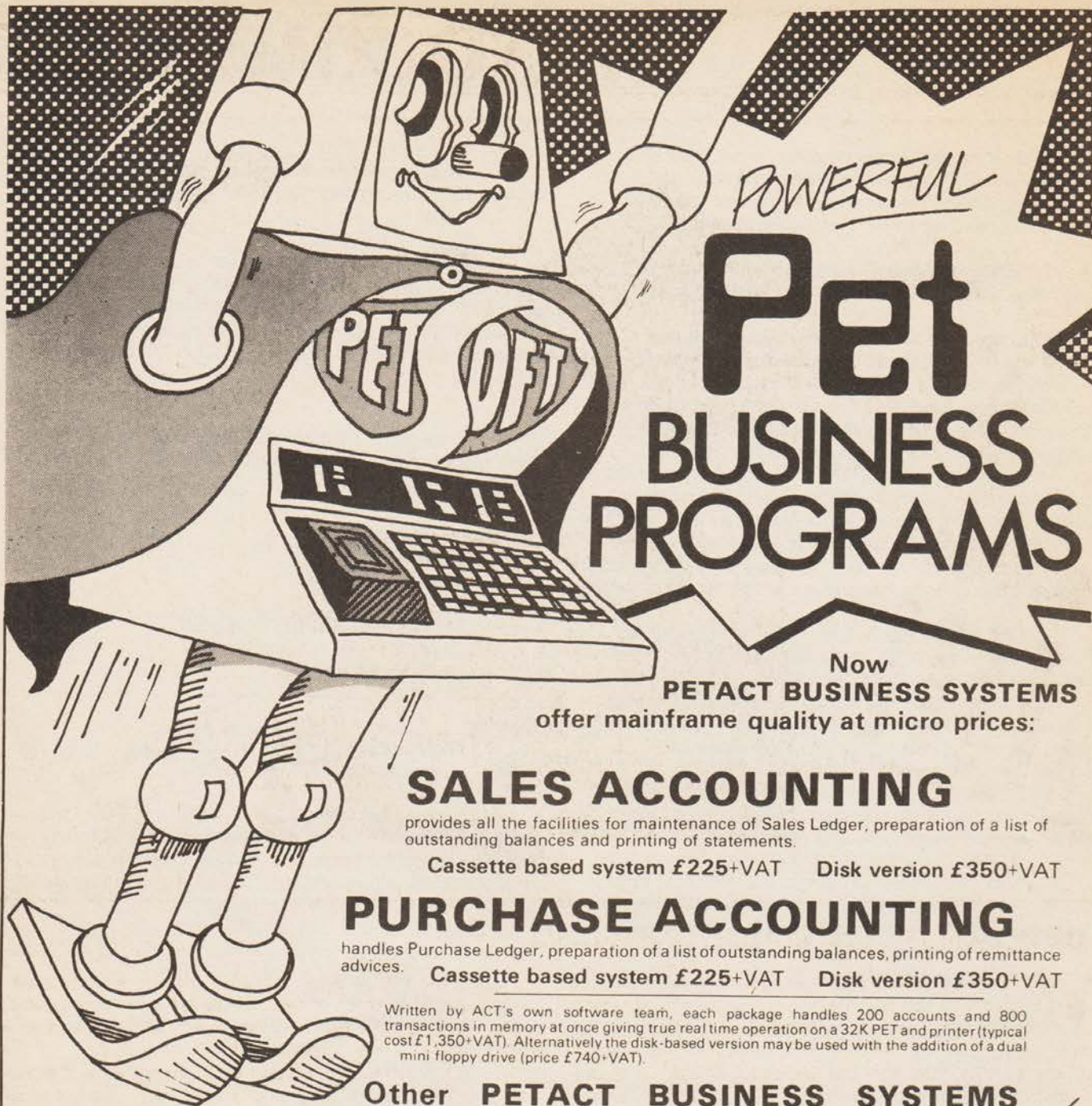
Have just received the June issue of CT and was pleasantly surprised to see the transformation from my rough notes to the printed version. There are however a few printing errors which, although trivial, may confuse some readers without the experience to distinguish them from the original text. I have shown these on a separate sheet in case you feel that such corrections should be pointed out in the next issue.

Yours faithfully,
A.P. Stephenson.

2 Kinloss Road,
Greasby, Wirral,
Merseyside L49 3PS.

ERRORS IN ARTICLE "D2 PROGRAMMING" (June Issue Computing Today)

- 1) Page 69, top right
c) IMMEDIATE ADDRESSING the symbol # precedes
- 2) Line 1 in all five programs has this symbol # missing before 00FF in the Assembly Column
- 3) Line 3 of Program 4 also has the symbol # missing before 03 in the Assembly column
- 3) The description below Program 2 applies to Program 3 and vice versa;
The most simple correction is to tell readers to mark the program "SWOP CONTENTS OF A AND B" Program 3, and the program "SWOP CONTENTS OF 26 and 27" to be marked Program 2
- 4) Line 3 of Program 5 has the symbol # missing before 05 in the Assembly column



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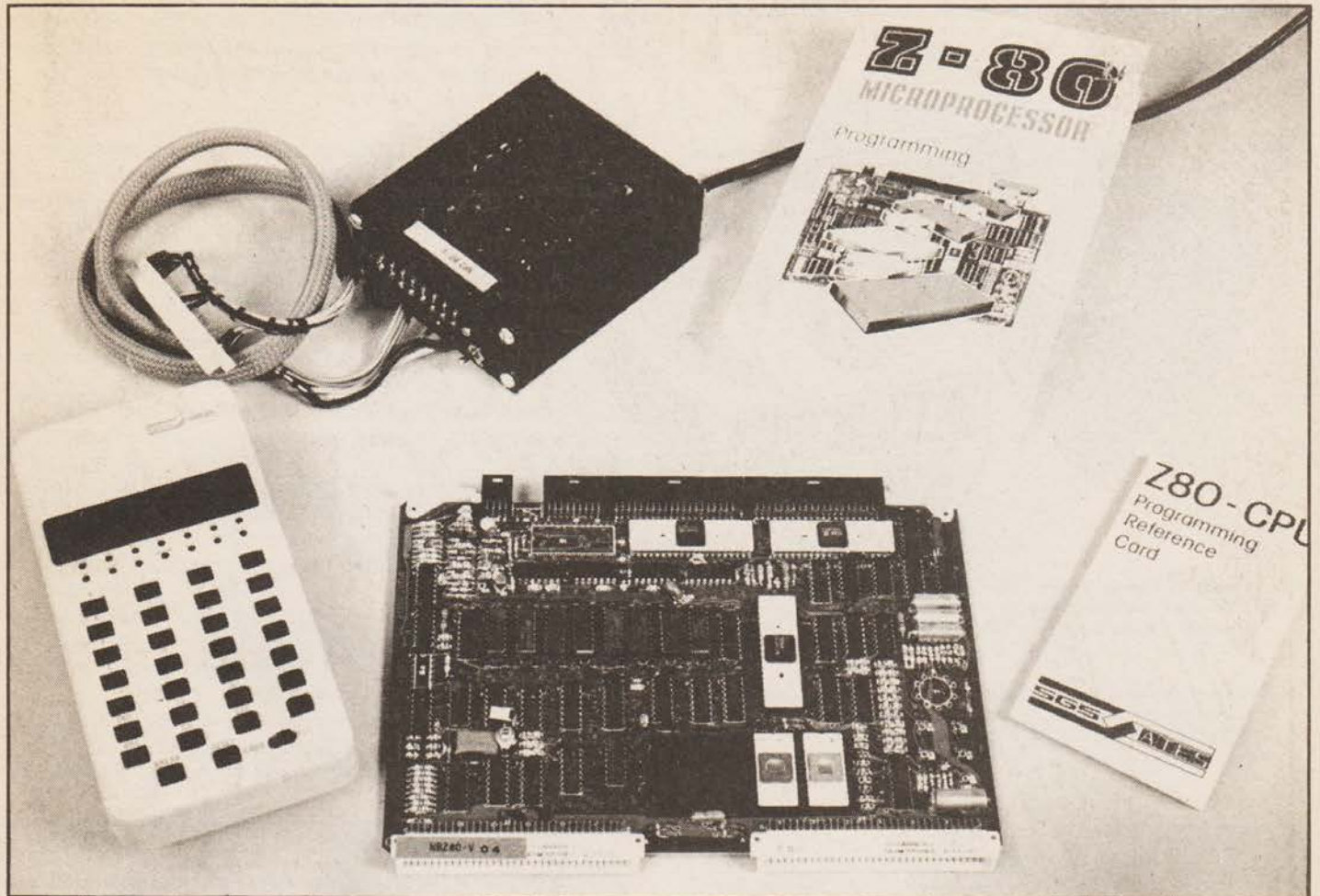
To **Petsoft**

My name is _____

My PET lives at: _____

5-6 Vicarage Rd., Edgbaston, Birmingham B15 3ES.
MY PET NEEDS FEEDING Please rush me a copy of your free 16 page catalogue of PET programs without obligation.

NANOCOMPUTER



A new Z80 based training system

One of the best ways to learn about micro-programming is by using an educational or training system. Normally these are either very expensive, Hewlett Packard's for example, or very basic like the ELF II or Acorn. The original exception to this rule was the Motorola D2 kit using the 6800 microprocessor but now there is a new system on the market which is called the Nanocomputer. Produced by the semiconductor firm SGS Ates it is designed to be used in the classroom or training environment but has the facility of being expanded to a full system.

It is based on the Z80 microprocessor from Zilog, one of the fast rising stars in the micro world and we decided to take a close look at this machine which will fill a large gap in the market.

Disaster Strikes

Our first attempt to use the system resulted in near panic as one of the RAM chips on the board expired, leaving us with a proverbial dead duck. This proved to our fault, most embarrassing, but the suppliers rushed us another system and all was well.

As we were using an early version of the machine we did not have either the card frame or the production keypad but even with the limited system we soon found out its huge potential.

Hardware Configuration

The board is of double sided construction with plated thru' holes and solder masked. All interconnections to the board

are made with high quality header sockets and no patches or lash ups have to be made. There are a number of vacant holes on the board, these are for later expansion and do not affect the performance of the system in any way.

The basic kit is supplied with a card frame that holds the processor board and power supply. There are slots available for the addition of an experimental kit, and one other card. The board is supplied with a 2K monitor in PROM, this can be upgraded to 8K by using the vacant sockets, and 4K of RAM which could be upgraded to 16K by changing over the chips. For connection to the outside world two Z80 PIO's are supplied, one taking care of the hand held keypad and the cassette, the other providing a general parallel interface.

The Operating System handles the input from the keypad or its replacement ASCII terminal at either 110 or 300 Baud, the cassette runs at 600 Baud. User programs are held in the on-board RAM and can be executed in either single step mode or at the full 2.5 MHz clock rate.

The hand held keypad allows any register of the Z80 to be inspected and modified, programs to be loaded and run, breakpoints to be set and the cassette to be controlled.

The Monitor also provides two test routines, one to check out the memory which is performed at every switch on and one to test out the displays on the keypad which can be run at any time.

Also supplied with the system were a set of circuit diagrams, the training manual and a quick reference guide to the Z80 codes. The quality of the documentation was high

but a fuller hardware explanation would have been rather nice, allowing an understanding of the internal structure of the processor as well as how to program it.

Start At The Beginning

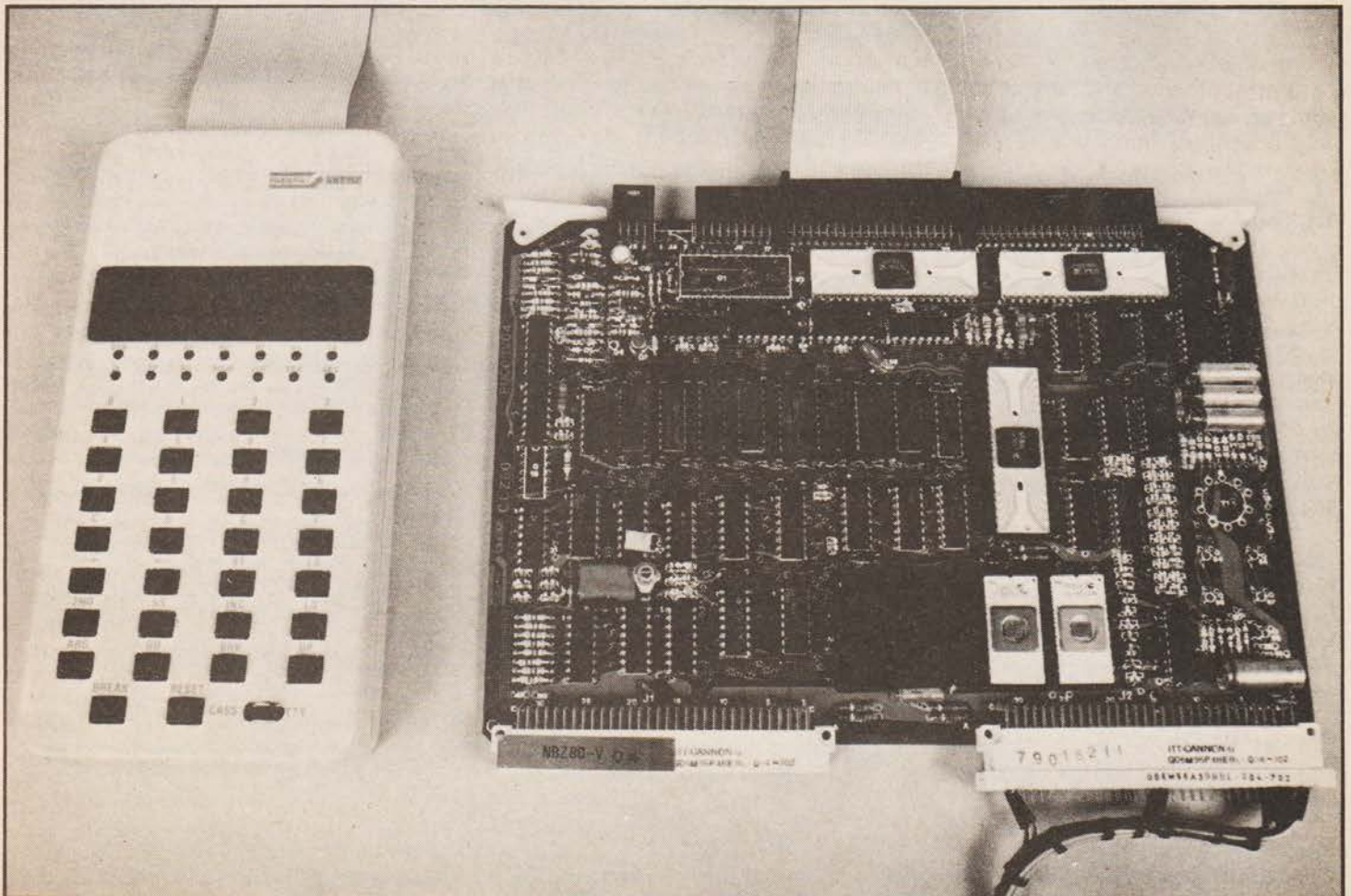
It is assumed that you have at least a basic understanding of Binary and Hexadecimal codes, the book covers them briefly, so you should have a good textbook to hand if you don't feel competent. The manual then goes on to explain the principles of how these codes can be used to program a microprocessor and gives a brief summary of the available commands for the Z80. It is important to read this section of the book as this is a training course, missing bits out is not a good idea. By the time Chapter 4 is reached you will have itchy fingers and this is where the real work begins.

The keypad, your only contact with the machine, is explained key by key and this section is probably the most essential of all. Having a processor but not being able to control it is rather a waste of time! Each section of the manual takes you through a set of instructions and is liberally interspersed with practical experiments in their use. By the time you have worked your way through the manual you will be more than prepared to tackle the Experimenters kit, which forms Part II of the course. Owing to the fact that we didn't have one we can't give you details of this but if the quality of the manual is of the same standard then it should be most impressive.

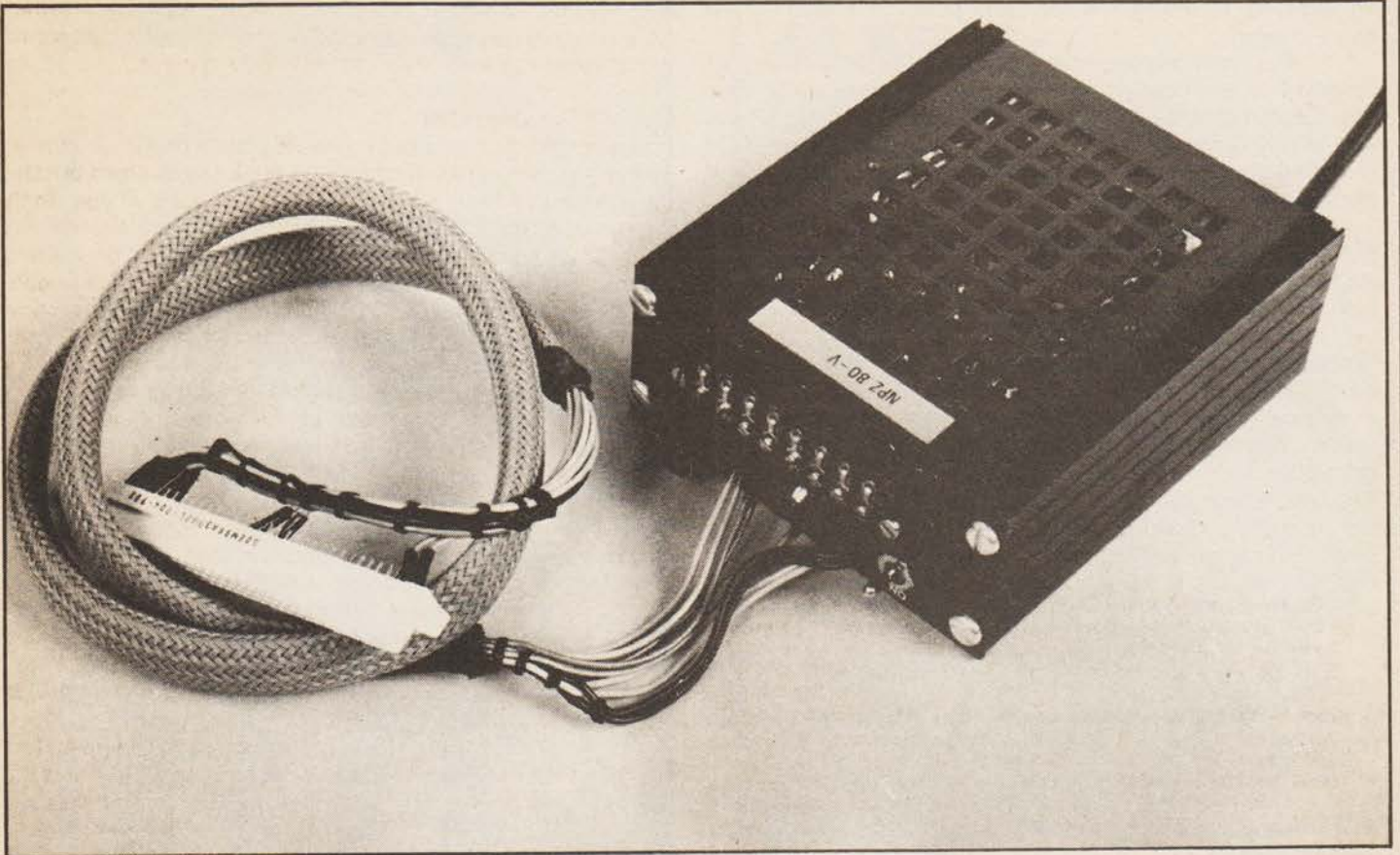
At the back of the manual are a variety of appendices giving a summary of the Z80 codes and other useful data. The only shortcoming of the book in our opinion was the

Opposite page:— the modular power supply that will normally be built into the Nanocomputer box, it supplies +5 and +12 volts to power the basic system. The expanded board will run from a single 5 V supply with on-board regulation.

Below:— the basic system. Several points of note, centre front of the board are the EPROM sockets for the upgraded monitor or BASIC, centre left are the RAM chips and the spare K note at the rear is for the extra VART. Note also that ceramic chips are used for the CPU and two PIO's.



NANOCOMPUTER



fact that although there are lots of example programs no demonstration programs are included. Even something as simple as counting up on the LED displays would have been most rewarding, mind you it should be quite possible for someone who has done the course to program it themselves!

Handling The Problems

The keypad supplied with the system that we reviewed, even though it was not the final version, was so flexible in operation that we decided to give it a paragraph or two on its own. Contained within the one unit are eight hex displays, for both address and data inspection, a hex keypad, twelve operation keys, reset and break keys, cassette or keypad selection switch and fourteen LED's to indicate the status of the device. The unit is connected via a 40 way ribbon to the main board, slightly inflexible in movement but of high reliability. The function of the hex pad is to load address and data information into the RAM. The mode of operation has to be selected first so the correct LED is set on by use of a pair of 'cursor' controls. Having selected say MEM in order to load a program you now input the starting address and hit the LA key. The address which was displayed on the right hand four hex displays now moves to the left hand set and the data stored in this location, if any, is shown on the right hand set. Memory locations may be stepped through by use of the INC key, allowing for checking of programs etc., but to load data the ST key is used and this automatically steps the memory location on by one. In order to load any of the register pairs the appropriate one is selected by use of the cursor and the first two digits entered by the keys. The key labelled 2ND is then used to shift this data to the high order byte of the pair and the low order byte is entered and ST is used to load it. Running a program is accomplished by

loading the starting address into the PC register and pressing GO. This causes the program to be executed at the full clock rate of 2.5 MHz. To single step a program the SS key is used, holding this key depressed causes the program to run at about one operation per second. Whilst the SS key is being used any register may be inspected. Breakpoints may be set in the program by use of the BRK key, LD and DP are used to load and dump to cassette, ARS is used to control the alternative register set and RESET and BREAK are self-explanatory. If one has never used a "pocket Teletype" before it will feel strange but you quickly get used to it, the key mnemonics are very helpful in this way. Overall the unit provides a powerful, low-cost method of interacting with the Nanocomputer and the slight re-design of the production unit makes it slightly less clumsy to use.

Upgrading The System

Apart from the first simple upgrade from the basic system to the Experimenters Kit you can take your Nanocomputer right up to a fully fledged machine. Several components are missing from the main board as we mentioned earlier, these can now be ordered and installed. Among the new pieces are a new software Monitor, the MO-Z, a UART which supports 50 to 9600 serial transmissions, a second cassette interface and a DC to DC converter which allows the whole system to be run off a single 5 V supply.

For future expansion memory cards are available in 16, 32 or 48K of RAM, a PIO with eight parallel eight bit ports and a serial I/O port as well as four timer/counter controllers. Cards are also available for VDU and keyboard control, floppy disks and PROM programming. All these additions plug in to a new card cage, and a more powerful power supply unit is required. A range of peripheral devices

NANOCOMPUTER

are available to utilize this increased power including a VDU and a printer.

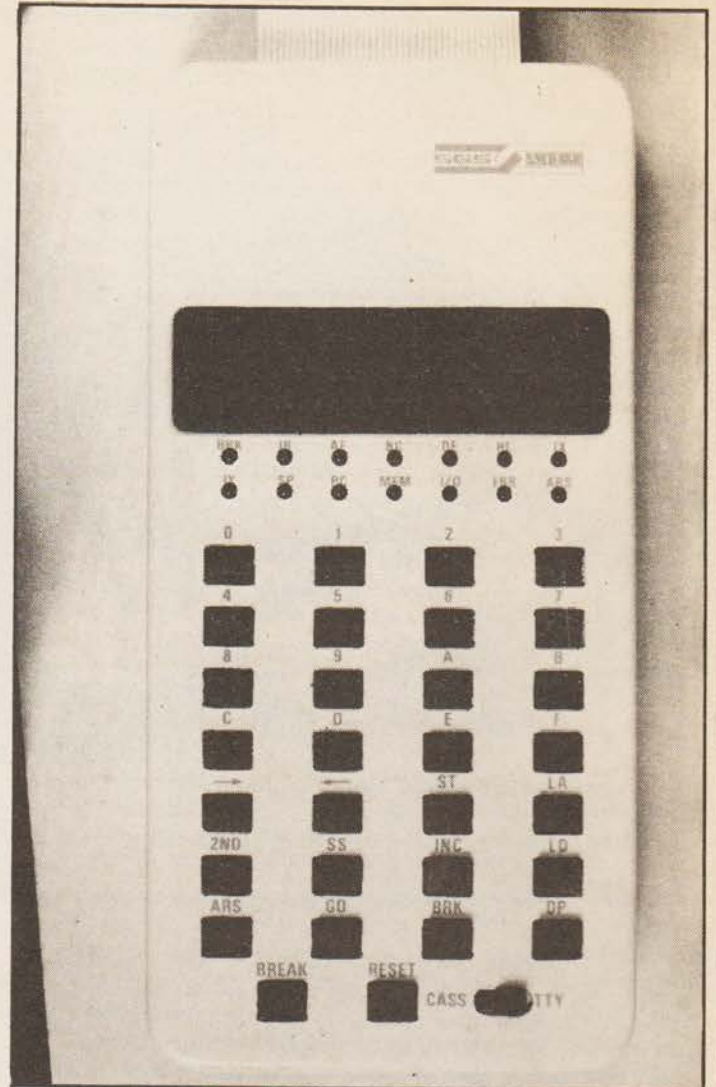
For your expanded programming needs a variety of software is available for the system including a 4K tape based Assembler, an 8K Monitor/Editor/Assembler in PROM and an 8K Control BASIC. The tape recorder is a specially modified audio recorder which is supposed to give enhanced performance and reliability.

Summary

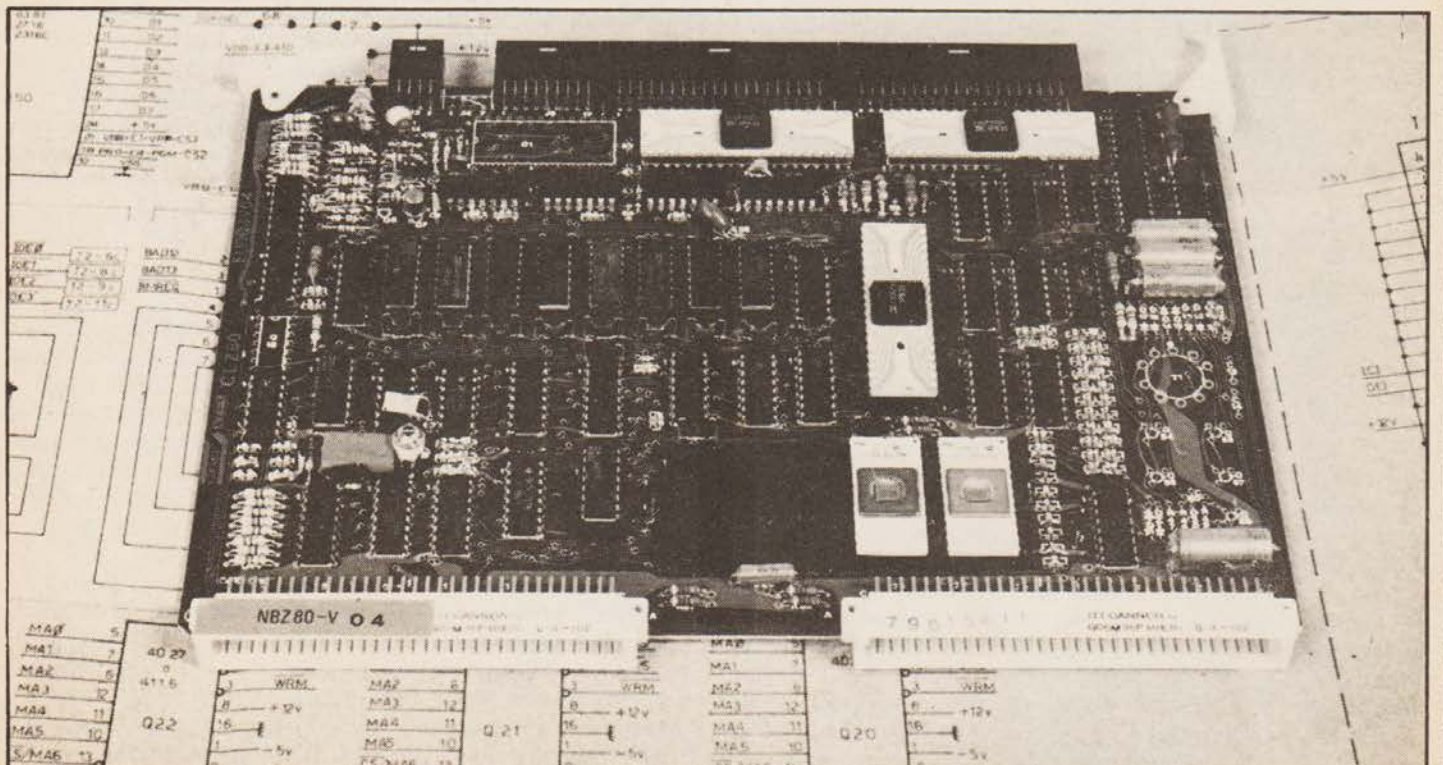
As the system is so versatile it is very hard to summarise on just the system that we had available to us. However we can say that the overall quality of both the hardware and the support was excellent. It is the first training system that we have come across that has been developed with the idea of integral expansion from the classroom to micro-computer system. Several others have attempted it but you always end up with a lash up of separate boards and other peripherals. The whole concept of the Nanocomputer appears to have been carefully thought out and with luck all the necessary parts for expansion will be available when required. The expected launch for the add-ons is in the Autumn but the basic systems should be available by the time you read this review.

Our thanks are due to Mr David Watson of the Midwich Computer Company. For further details of the systems availability you should contact him at Hillsborough House, Churchgate Street, Old Harlow, Essex, or telephone on 0279-25756.

The price of the basic system without a power supply is £260 and the Experimental Station is £430. Both prices are exclusive of VAT.



Top right:— the prototype keypad unit, the production versions are black and have re-arranged keys. Below:— the basic board with its circuit diagram.



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CHESS CHALLENGER - £85.65 + VAT. PLAY CHESS AGAINST THE COMPUTER.

The stylish, compact, portable console can be set to play at seven different levels of ability from beginner to expert including 'Mate in two' and 'Chess by mail'. The computer will only make responses which obey international chess rules. Casting, on passant, and promoting a pawn are all included as part of the computer's programme. It is possible to enter any given problem from magazines or newspapers or alternatively establish your own board position and watch the computer react. The positions of all pieces can be verified by using the computer memory recall button.

Price includes unit with wood grained housing, and Staunton design chess pieces. Computer plays black or white and against itself and comes complete with a mains adaptor and 12 months guarantee.

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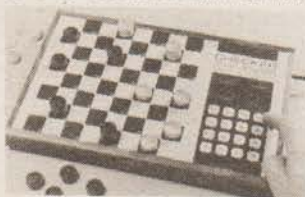
A special bulk purchase of these amazing chess teaching machines enables us to offer them at only £19.75 less than half recommended retail price. The electronic chess tutor is a simple battery operated machine that can actually teach anyone to play chess and improve their game right up to championship level. This machine is not only for total beginners but also for established players wanting to play better chess. Unit contains the electronic chessboard with 32 chess pieces, a 64 page explanatory booklet and a set of 32 progressive programme cards including 6 beginners cards, 16 check mate positions, 9 miniature games, 5 openings, 3 end games, 28 chess problems and 2 master games.

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The workings of the PET IEEE 488 bus explained

The familiar PET home computer possesses one of the real oddities in the microcomputer world. The user is presented with not a true bus but a version of the all singing, all dancing IEEE-488 instrumentation data bus. The original PET manual was very vague on the structure and use of this, we have set out to try and clear up some of the mysteries. The very fact that the PET is provided with a user port at all means that it must be useable, and indeed there are several commercial interface adaptors available, but the average amateur's response seems to be one of panic when hardware design is suggested.

The one vital phrase that is buried in the manual is as follows, "as implemented on". A rather better wording for this is "as adapted for" because the IEEE-488 bus on PET is a subset of the original standard. Armed with this vital piece of information we will now try to give you the rest of the information you will need.

The Bus Structure

The bus can be divided into three sections, to make it simpler:—

1. Data bus
2. Transfer bus
3. Management bus

These three sections all interact with one another in specific ways, and it is the understanding of these interactions, handshakes as they are often called, that allows interfaces to be designed.

The data bus is an eight line bi-directional highway. The lines are designated DI01 to DI08, and are active low. The normal status of the line is therefore high and any device which grounds a line puts data onto it. The data is transferred in bytes and the most significant bit is on data line DI08.

The Transfer Bus performs all the handshaking and thus controls the transfer of data on the bus. The handshaking sequence is devised so that the slowest device will always complete a transfer once it has been initiated, if it tried to do it without controls data would be lost. There are three lines in the transfer section, NRFD, DAV and NDAC. The order of handshaking is shown in Fig 1. We will have to take a closer look at each. NRFD (Not Ready For Data) is only high when all "listeners" are ready, if any device is not ready the line is low. This allows a slow device to hold everything up, protecting its data integrity. The line is used for devices that send on the bus "talkers" in IEEE jargon. DAV (Data Valid) is put low to enable "listeners" to take data from the bus. The line can only be put low when NRFD is high, in other words all "talkers" must wait for "listeners". NDAC (Data Not Accepted) is held low by a "listener" until it has taken the data off the bus. When this goes high a "talker" can change the data on the bus.

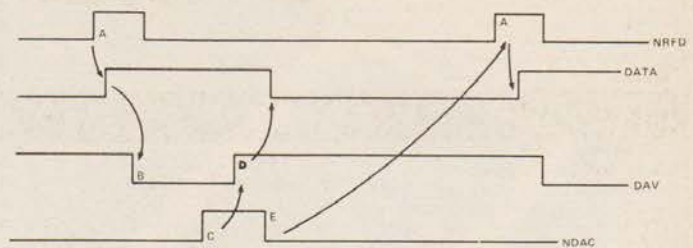


Fig 1. The handshake timing diagram.

The Management Bus consists of five lines, only two of which are fully implemented on the PET. These two are ATN (Attention) which is set low for device assignment. If it is low then the bus is carrying addresses of peripheral devices and control messages, if high only assigned devices may transfer data on the bus. The second line is EOI (End Or Identify) and can be optionally set low by a "talker" at the end of a data transfer. However the controller always sets EOI low during the last byte transferred. The other three management lines are SRQ (Service Request), IFC (Interface Clear) and REN (Remote Enable), and are not really of interest to us.

We have summarized all the controls and interface lines in Table 1 along with their connections.

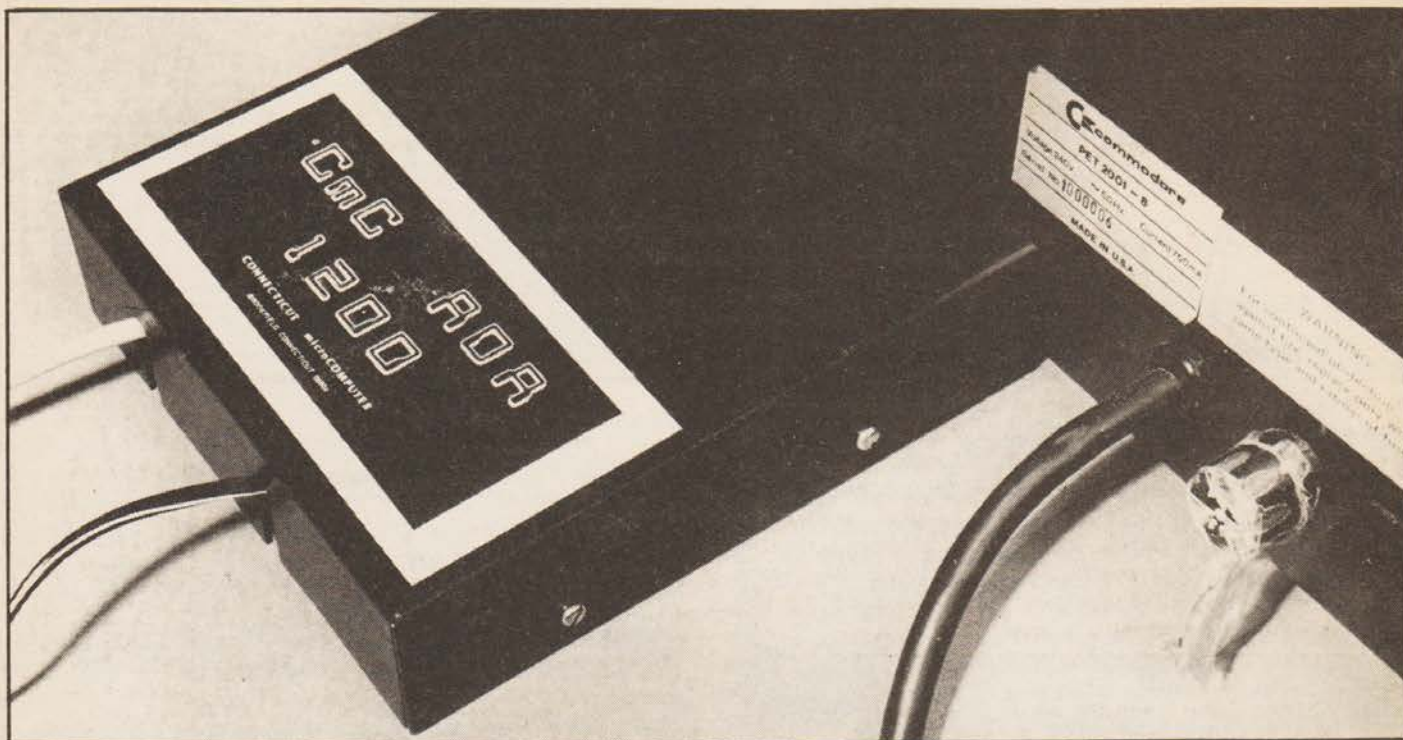
Handshaking Routines

Because the IEEE bus was primarily designed for instrumentation rather than for home computers the handshake signals are fairly easy to use. Figure 1 shows a typical handshake taking place, the timings are relative and not drawn to scale. At "A" NRFD is set high to signal the listener that the talker or talkers on the bus are ready to send data. This line will normally be set at switch on. The talker will now place data

Pin	Designation	Function
1	DI01	Data 1 (LSB)
2	DI02	Data 2
3	DI03	Data 3
4	DI04	Data 4
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready For Data
8	NDAC	Data Not Accepted
9	IFC	Interface Clear (optional use)
10	SRQ	Service Request (optional use)
11	ATN	Attention
12	Chassis Ground	
A	DI05	Data 5
B	DI06	Data 6
C	DI07	Data 7
D	DI08	Data 8 (MSB)
E	REN	Remote Enable (optional use)
F		
H		
J		
K	Ground	
L		
M		
N		

Note:— polarization slots occur between 2 and 3, 9 and 10.

Table 1. Bus lines and edge connector terminations.



CMC interface adaptor for the PET bus.

on the lines, when it is ready to do so. At point "B" the talker will set DAV low to indicate to the listener that the data on the lines has settled and is valid to read. As soon as one listener has accepted the data that listener sets its NRFD line low. If there is more than one listener the slower ones set their NDAC high, when all have taken their data NDAC is then asserted high. This occurs at point "C" on the timing diagram. The talker now sets DAV high, point "D", indicating that the data is no longer valid. The listeners respond to DAV going high and set NDAC low, point "E", and NRFD may now be reset high ready for the next handshake. There are only two timing constraints for the PET, if it is acting as a listener then it expects DAV to go low within 64 mS of it setting NRFD high. When PET is acting as a talker it then expects NDAC to go high within 64 mS of it setting NRFD high. In other words the data should be read from the lines within 64 mS in either direction.

There are several other observations to be made about the handshake. We have not covered the ATN line at all, this is set high for data information on the bus, low for address information. We will obviously have to take care of this in any interface we design as we are not interested in any addresses or control signals.

Using The Bus

Most of you who have the PET will have become familiar with LOAD and SAVE commands for the cassette and will be wondering how to use the bus for these purposes. The bus actually looks like a data file to the PET BASIC and one has to use file commands to access it. The following commands are used:—

OPEN, CLOSE, PRINT#, INPUT#, GET#, CMD and ST.

To output from the PET one has to open a file and this is done in the format:—

OPEN (Address), (Device), (Secondary Address), "Filename"

The Address is within the region 1 to 255 and must be referenced by the CLOSE, PRINT#, INPUT# and GET# statements.

The Device is the address of the physical device on the bus and must be in the range 4 to 15. A Secondary Address is only sent on the OPEN and CLOSE commands and is normally ignored. The command PRINT# sends ASCII characters to the bus, INPUT# receives characters from the bus under BASIC rules, GET# "gets" a character or digit from the bus. It should be noted that all these commands refer to the Address specified by the OPEN statement. Using the CMD command allows output from BASIC to be sent to a device specified in a previous OPEN command. This allows program listings to be obtained and also leaves the bus active, hence allowing more than one "listener" on the bus. Access may be obtained to the status of the bus by inspecting the BASIC variable ST. The bits and their mask codes and interpretation are to be found in Table 2. A command of the form:—

IF (ST) AND MASK THEN. . . (Where MASK is either 1, 2, 64 or 128)

This test should be done immediately after the I/O operation that the user is interested in.

Getting On The Highway

The hardware details of the bus are very simple, as rather than put a flashy IEEE connector on the back of PET an edge connector is used. This can be seen in Photo 1 and also in Fig 2. It is a 12 position 24 contact (ie double-sided) edge connector with 0.156" pitch and can be obtained from most PET stockists. Typical manufacturers are AMP, CINCH and Sylvania but at a pinch you can cut down a larger type.

PET BUS

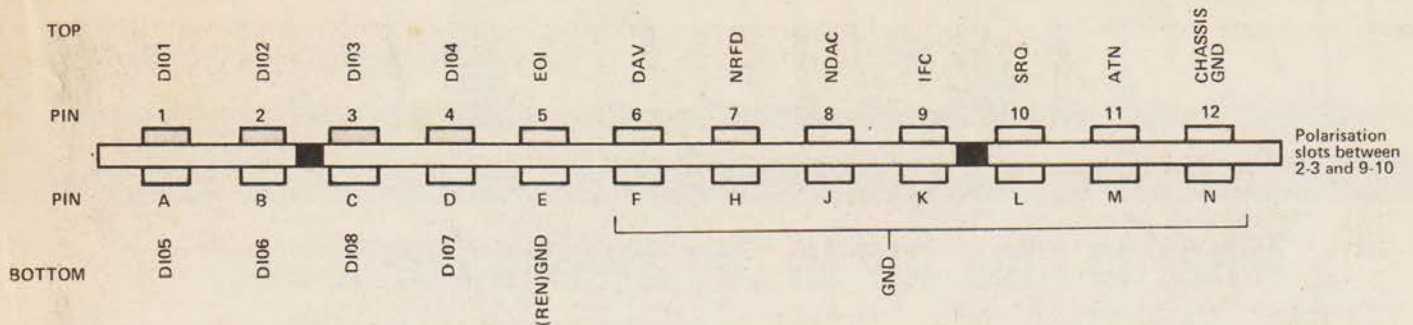
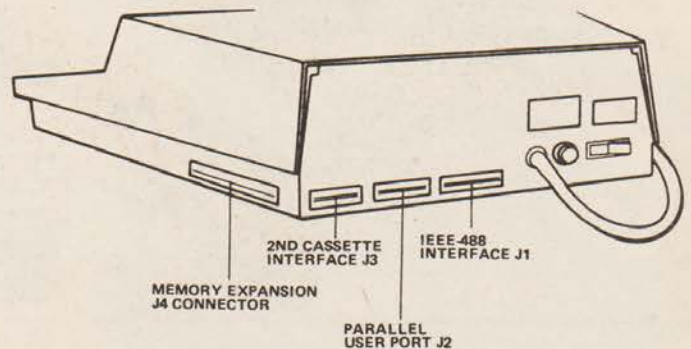


Fig 2. The PET rear edge connector.

There are some electrical limitations which must be observed, or else you may have problems. The cable should be no longer than 20 metres, devices should be spaced less than 5 metres apart. The number of devices on the bus should be limited to 15 and the data transfer rate kept to below 250KHz, although with tristate drivers you can push it up to 1MHz. As a design recommendation all bus lines on your interface should be buffered, this solves a lot of those inexplicable problems that tend to arise.

Bit	Mask	Status
0	1	Time out on data transfer, response longer than 65ms
1	2	Read error, DAV not sent within "time out"
6	64	EOI
7	128	Device not present, return to BASIC

Table 2. Status word codes and interpretations.



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Until last month very few people had even heard of the LM10. In a few more months not having done so will be a bigger disgrace than supporting Chelsea. Ray Marston produces one of his special features to help you out of the second division next month, so don't miss it.

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No it's not Dolby. It is based on a brand new chip set from National. It has an amazing low component count. It turns in a very respectable 'sound' and is ideal for home usage. It is inexpensive and a very good reason to buy ETI next month.

Interfacing made easy

An input/output port must provide a versatile programmable interface between the microprocessor and the external system devices (peripherals). Since the "devices" can vary from simple lamps, switches or keyboards to paper-tape readers, punches, visual displays, XY recorders etc. it is understandable that a price must be paid for such versatility. The MC6821 Peripheral Interface Adapter (PIA) is certainly versatile but its architecture and personality reflects the data sheets supplied with it—cold, logical and aloof. Once this data is deciphered and confidence is gained, the PIA will be accepted as a well designed little box and surprisingly easy to program.

Relationship Between PIA And MPU

There are no special instructions for the PIA because, as far as the 6800 MPU is concerned, it appears as a block of four "memory addresses" which can be read from or written into like any other RAM. These addresses can be chosen arbitrarily when wiring up the system providing they occupy four consecutive addresses. In Figure 1, these addresses have been chosen as 8004, 8005, 8006 and 8007 in order to correspond with the Evaluation Kit (D2) supplied from the makers. The eight data lines of the PIA are simply connected to the MPU data bus as normal and it will be noticed that several control lines are also connected between the two.

External Interface Lines

Except for subtle differences to be explained later, the PIA can be considered as two identical halves, side "A" and side "B", each half having eight data I/O input lines and two special lines used for control or "handshake" purposes. To avoid repetition, discussion will be limited to the "A" side and it can be assumed that the "B" side will behave in the same way.

PA0 to PA7 — are the data I/O lines any of which can be used as either an Input or an Output depending on how the programmer writes the initialisation routine. Thus we can have say three behaving as Inputs and five as Outputs, a most useful property.

CA1 and CA2 — are the peripheral control lines. CA1 is always an Input but CA2 can be initialised as an Input or an Output.

The Internal Registers

There are three registers in each half:

a. Data Register

This is the buffer between the I/O lines and the MPU data bus and after initialisation is available to the programmer as "Address 8004" (8006 for B side).

b. The Direction Register

It was stated earlier that the I/O lines can be inputs or outputs. The direction register is used to decide this by the rule,

"0" = input ; "1" = output

Thus if this register is initialised with the pattern 00001111 (0F hex) then PA0, PA1, PA2 and PA3 would behave as outputs and

the rest as inputs. It is available to the programmer as "Address 8004" (8006 for B side). This is rather surprising because it is the SAME address as the data register!

c. The Control Register

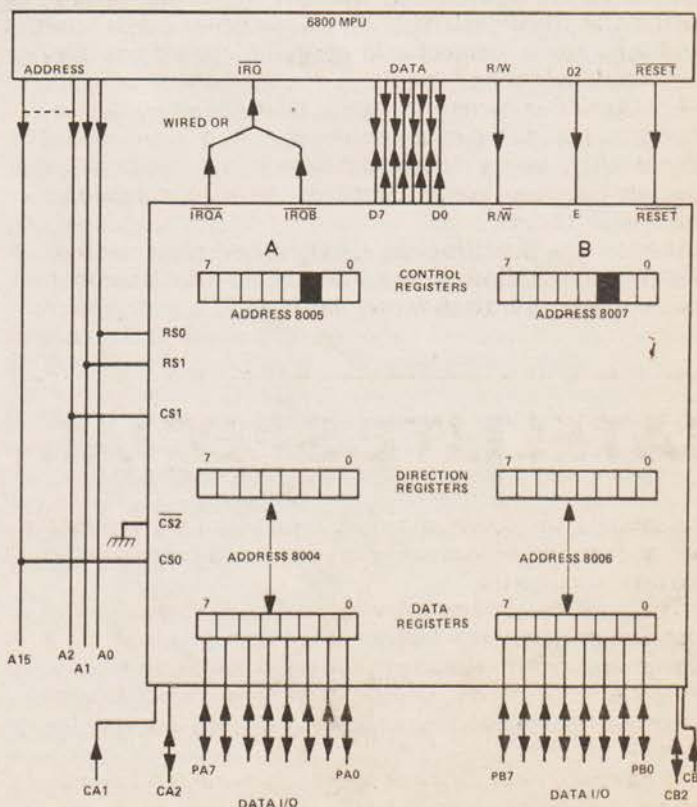
This is the register which causes some anxiety to the newcomer because it is a hotch potch of various bits, each having a separate functional identity. (If it is any consolation, it caused the writer more than anxiety—apoplexy in fact).

Although full details will be attempted later, only bit "2" is important at this stage (shown dotted in figure 1), because it is this bit which dissolves the discrepancy of two registers having to share the same address.

When bit "2" is 0, the address 8004 belongs to the direction reg. When bit "2" is 1, the address 8004 belongs to the data reg. The control register is available to the programmer as address 8005 (8007 for B side). The remaining bits are all concerned with the behaviour of the control lines CA1 and CA2, a torture to come later.

The allocation of the addresses are cunningly thought out. Under system reset conditions, all registers in the PIA are reset to zeros—which includes the bit "2" in the control register. So the first time address 8004 is used, it will address

Figure 1 The PIA and its relation to the MPU.



the direction register. After this the programmer will ensure that bit "2" is set to 1, so subsequent reference to 8004 will address the data register. It would be most unlikely to have to change the direction register contents in the same program, but if so, it would be necessary to clear bit "2" first and reset it again afterwards.

Connections To The Address Bus

The PIA behaves as four memory locations, so it must be similar in some respects to conventional memory chips in the manner of connection to the main address bus of the MPU. Thus we must expect to find address lines to pick out which location within the chip and other lines which select the chip itself.

There are five lines from the PIA to the MPU address bus, two Register Select lines (RS0 and RS1) and three Chip Select lines (CS0, CS1 and CS2). Note from Figure 1 that RS0 and RS1 are driven by the two lowest order address lines A0 and A1 which ensures that the four internal locations have consecutive address codes.

The chip select lines must ALL be enabled in order to bring the PIA on-line. Thus CS0 and CS1 must both be HIGH and CS2 must be LOW. The arrangement shown in figure 1 is deliberately naive to simplify the appearance for the purpose of understanding the basic ideas behind "chip select". Thus CS2 is shown connected to ground ensuring this line is enabled. CS0 will only be enabled when address line A15 is HIGH and A2 must be HIGH to enable CS1. Taking the four perms of A0 and A1 as 00, 01, 10 and 11, it may be seen (with a bit of mental effort) that the four hexadecimal codes 8004, 8005, 8006 and 8007 are established as active addresses for the PIA registers. Unfortunately, there will be thousands of other address combinations which will also activate the PIA because the twelve wires unused out of the sixteen can be 1s or 0s; thus the address code FFF4 will have the same effect as 8004, so will C004, ABC4 etc etc. Now if the PIA was the only other chip apart from the MPU itself, this wouldn't matter much but of course there would be RAM and ROM chips each competing for a unique band of addresses. However, it is easy to modify Figure 1 to increase the "exclusivity factor" of the PIA addresses. For example, the ground return of CS2 could be replaced by say an OR gate as shown in figure 2.

Only when every input to the OR is a "0" will CS2 be enabled so the range of addresses is severely limited (apart from A12, A13 and A14 which are still don't-care lines). Of course if you have bought a complete Evaluation or Development kit, the foregoing details have all been taken care of but there is always the possibility that an extra or perhaps several extra PIAs are required for a particular project so it is as well to have some familiarity with address decoding principles. Although unlikely, it would be possible to connect say, 1000 PIAs to the address bus which would allow a total of 20,000 peripheral lines to play around with. These would still only occupy 4,000 addresses out of the total of 65,536 possible. One word of warning, if such grandiose schemes are to be considered the poor old address and data buses will require some additional "Bus Driver ICs" to handle the accumulated leakage currents.

Control Lines To The MPU

Enable (E) is the timing control, usually connected to the 02 clock line of the MPU. Even with the correct address lines enabled, the PIA is not viable until the E pulse goes HIGH. (When we later discuss the Control register bits the E

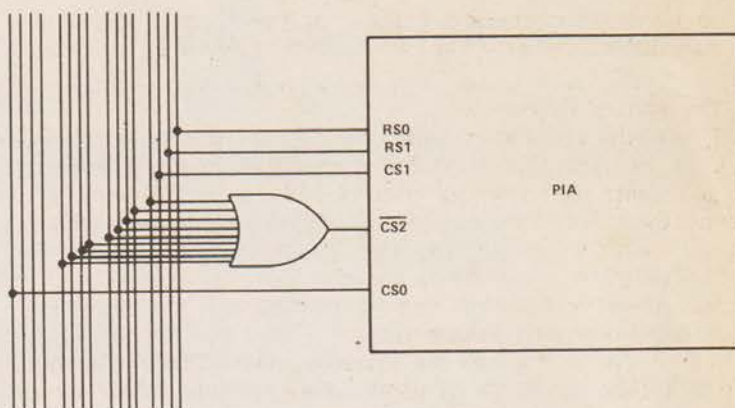


Figure 2 Alternative chip select arrangement.

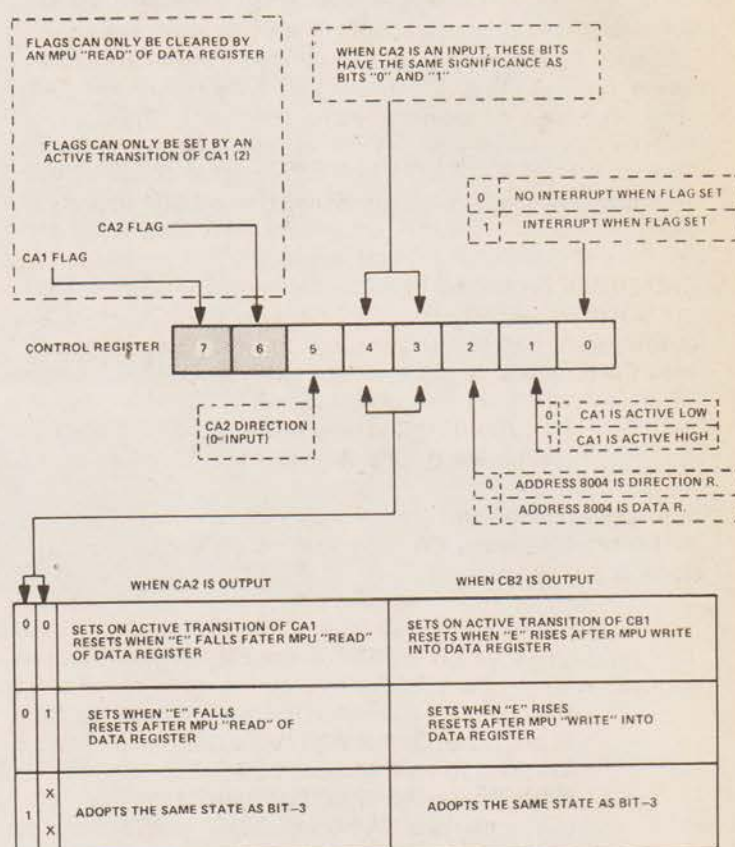


Figure 3 Programming the PIA control registers.

RESET pulse level will be found important). When this is driven LOW, by say a momentary pulse from a push-button, the six registers of the PIA are cleared to zero.

Read/write (R/W) The state of this line decides whether the MPU is reading from or writing to the PIA registers. The "normal" state is HIGH (read) and LOW (write).

INTERRUPT REQUEST (IRQA and IRQB) inform the MPU that a peripheral line is asking to interrupt the present program and cause a jump to another program called the "interrupt routine". Unfortunately, there is only one IRQ input on the MPU which means that the A and B side interrupt requests must be wire-ORed, implying that there is

no hardware distinction between the two sides. This is no real obstacle because they can be distinguished by software.

The Control Register

This is the brute that causes most of the misery. Each bit, with the exception of bit-2 mentioned before, has something to do with the behaviour of the peripheral control lines CA1 and CA2. Motorola issue a very informative diagram which, to an expert programmer, reveals all. Figure 3 attempts to "simplify" this diagram although it still presents a rather depressing appearance, requiring a bit by bit discussion before it begins to make sense.

The definitions are in terms of the PIA A-Side but the B-Side behaviour is identical except when CB2 is an output.

a. The two FLAG bits

These are best got out of the way first because these are the only two which cannot be set by instructions in the program. Bit 7 can only be set by a signal from the outside world arriving via CA1; bit 6 can only be set via CA2 (when it is defined as an INPUT).

Once set, they can only be cleared by the next MPU read of the DATA REGISTER. Example: if either of the two flags are set, the instruction LDA A 8004 will clear them.

b. CA2 DIRECTION (bit 5)

Bit 5 determines whether CA2 behaves as an input or an output according to the same rule previously encountered with the direction register:

If bit 5 is a 1, CA2 is an output
If bit 5 is a 0, CA2 is an input

c. Interrupt bit (bit 0)

If this bit is 1, when CA1 flag is set the interrupt request signal is activated.

d. CA1 Active-level (bit 1)

This bit decides which EDGE of the CA1 signal sets the flag, according to the rule:

If bit 1 is 0, CA1 is ACTIVE LOW
(flag sets when CA1 goes LOW)
If bit 1 is 1, CA1 is ACTIVE HIGH
(flag sets when CA1 goes HIGH)

This is very useful because some peripheral devices are normally HIGH and go LOW when active, others are opposite in behaviour.

e. Bits 3 and 4 when CA2 is an input

These two bits are very nasty because their function is different according to whether CA2 is defined as an input or an output. When CA2 is an input, they behave exactly the same as bits 0 and 1 except the flag is the CA2 flag. Thus bit 3 will be the interrupt bit for the CA2 flag and bit 4 will determine the CA2 active level.

f. Bits 3 and 4 when CA2 is an output

Figure 3 shows the possibilities. Perhaps the strangest perm is when bit 4 is a 1 because we can imagine that bit 3 is physically connected to CA2. Thus if bit 3 is 1, CA2 is HIGH; if bit 3 is 0, CA2 is LOW. Thus we can say that when bit 4 is held at 1, CA2 will "follow bit 3".

In this mode, CA2 behaves as a 9th I/O output line which can be made HIGH or LOW by programming bit 3 accordingly.

Initialisation Examples

"Initialising the PIA" refers to the few instructions, normally at the head of the program which loads the correct bit patterns in the direction and control registers. The patterns must first be set into a register (accumulator or index register) using immediate addressing and then storing in the appropriate PIA locations. Because the direction and control registers always occupy consecutive addresses it is both convenient and economical to utilise the double length Index Register to kill two birds with one stone.

For example, supposing the pattern 00001111 (0F hex) is to be placed in the A side direction register and the pattern 0000100 (04 hex) in the control register. Assuming the address allocations as shown in Figure 1, the initialisation would proceed as follows:

```
CE 0F 04    LDX #0F 04  (# means immediate address)
FF 80 04    STX  80 04
```

This is easily understood when remembered that when storing the Index Register the higher order byte (0F) goes in the address quoted and the lower order byte (04) in the next higher address. The following examples should be studied:

Example 1

PA0, PA1 and PA3 to be inputs and the remaining five to be outputs. CA1 and CA2 not required. All eight lines PB0 to PB7 to be outputs. CB1 and CB2 not required.

The initialisation is as follows: 11111000 in 8004, 00000100 in 8005, 11111111 in 8006 and 00000100 in 8007.

```
CE F8 04    LDX #F8 04    A side
FF 80 04    STX  80 04
```

```
CE FF 04    LDX #FF 04    B side
FF 80 06    STX  80 06
```

Note: only bit 2 is important in the control registers, the remaining bits are "don't care" so, for reasons of simplicity, are made 0s.

Example 2

PA0 to PA7 to be outputs. CA1 to be active LOW input without interrupt request. CA2 to be active HIGH input with interrupt request. PB0 to PB7 to be inputs. CB1 to be active HIGH input with interrupt request. CB2 to be active LOW input with interrupt request.

Initialisation: 11111111 in 8004, 00011100 in 8005, 00000000 in 8006 and 00001111 in 8007.

```
CE FF 1C    LDX #FF 1C    A side
FF 80 04    STX  80 04
```

```
CE 00 0F    LDX #00 0F    B side
FF 80 06    STX  80 06
```

Example 3

PA0, PA1 and PA2 to be inputs, the rest outputs. CA1 to be active LOW input without interrupt request. CA2 to be

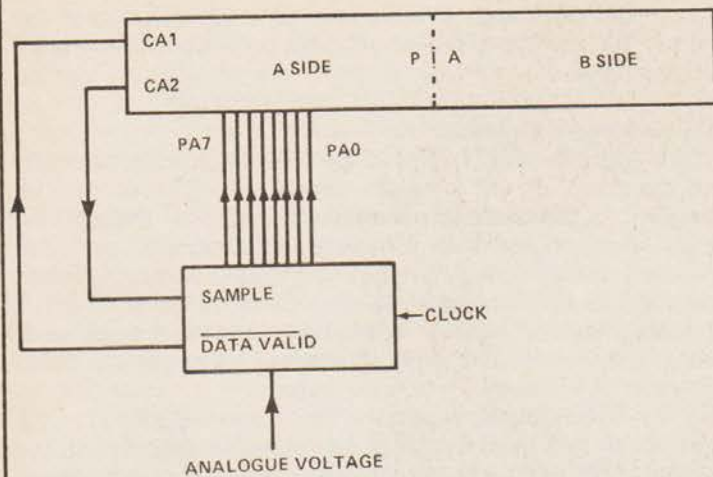


Figure 4 Interface to A/D converter.

output which adopts the same state as bit 3 in the control register.

PB0 to PB7 to be outputs. CB1 to be active HIGH input with interrupt request. CB2 to be output which is set HIGH when the CB1 flag sets HIGH and is cleared after the next STA 8006 instruction.

Initialisation: 11111000 in 8004, 00110100 in 8005, 11111111 in 8006 and 00001111 in 8007.

CE F8 34	LDX #F8 34	A side
FF 80 04	STX 80 04	
CE FF 27	LDX #FF 27	B side
FF 80 06	STX 80 06	

Example 4

As example 3 above but assuming it applies to a second PIA with new addresses as follows: A side Direction Register at 6000, Control Register at 6001; B side Direction Register at 6002, Control Register at 6003.

CE F8 34	LDX #F8 34
FF 60 00	STX 60 00
CE FF 27	LDX #FF 27
FF 60 02	STX 60 02

Example 5

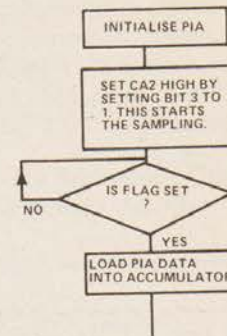
To introduce a more practical bias, we shall assume an 8 bit resolution Analogue to Digital Converter IC is to be connected to the A side PIA with interface lines as shown in Figure 4.

Action: On receipt of a pulse to "SAMPLE" (a HIGH), the A/D conversion count commences. When the correct count is reached, DATA VALID goes LOW indicating the digital outputs are truly representing the analogue input voltage. Assuming interrupt is not to be employed, then it is clear that PA0 to PA7 must be inputs, CA1 must be active LOW and CA2 can be made to follow bit 3 (although the latter is only one of the possible solutions).

A suitable initialisation could proceed as follows:

CE 00 34	LDX 00 34
FF 80 04	STX 80 04

Note that the initialisation will leave CA2 LOW (inactive). The rest of the program must monitor CA1 flag bit and set bit 3 HIGH again after the valid data has been read from 8004 into one of the accumulators. The following flow chart may be useful in appreciating the overall scheme:



How can we tell if the flag is set? By loading the control register into an accumulator and testing if it is a negative value (CA1 flag is at bit 7 so it is interpreted as the sign bit when in the accumulator).

Input And Output Drive Requirements

Full details are given in the PIA data sheets and should be consulted when contemplating any serious design. However, the "detail" can be a little frightening at first sight so the following broad outline may help to break the ice:

A SIDE I/O DATA LINES
When inputs: behave as one standard TTL load. CA1 similar
When outputs: can drive one standard TTL load
B SIDE I/O DATA LINES
When inputs: behave as high impedance tristate inputs drawing only 2 uA typical when driven HIGH or LOW.
When outputs: can drive one standard TTL load, but can deliver 2mA5(typical) 1 mA(minimum) at 1V5 in the HIGH state. CB2 also has this power when output.

Note the B side has greater possibilities than the A side. For example it can easily supply the minimum 1V2 necessary to drive a Darlington pair at a comfortable 1 mA or more.



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Making Effective Use Of The PIA

Although there are twenty external interface lines on the PIA, it is easy to run out of wires unless a stern frugal attitude is adopted. Every one of them must be made to pull its weight to the full; the alternative could be the purchase of a second (or third) PIA which apart from the cost, places an extra load on the address bus and wiring time. It is easy to develop a kind of mania for software. For example, there is little point in writing twenty or more bytes of code to "save" the use of a 7490 counter (costing about 30p) simply to satisfy the ego of a microprocessor purist. A well designed system should render unto Caesar the things that are Caesar's and to the ROM the things that are ROM's! The distribution of hardware and software should be a common sense exercise free from predetermined bias.

There is of course a danger in the other direction; if there is too much hardware and too little software the obvious conclusion is that a microprocessor was not required and the system could have been implemented by a completely hard wired black box. It is a good plan to reject out of hand the first solution that comes to mind (even if you eventually return to it in the end). Letting the problem simmer in the mind for a while can often lead to a flash of divine inspiration—called "lateral thinking" by the Mid Atlantic fraternity—which could save you ½K of ROM in return for a couple of TTL chips.

The word "system" has been mentioned above and to those readers who use microcomputers only for number crunching or games or filing systems, requires some explanation. Any computing system can be considered as a closed loop "servo mechanism" in which the computer input and output is "closed" by the external peripherals. For example, a computer connected to a conventional teletype receives input from the keyboard and outputs a "correction" to the print mechanism. A simple VDU with keyboard behaves in a similar fashion. There is however a wide range of activities which can be controlled by a microcomputer in addition to the conventional data processing role. Model Railway enthusiasts for example can increase the sophistication of the operating system by using a microprocessor as the controller, keen gardeners with a scientific bias can arrange a perfect green house environment throughout the year, the family car can have its instrument panel transformed into a futuristic (and impressive) panorama of winking warning lights and LED digits vomiting out data on gallons per mile, engine noise level, gradient of road etc etc.

These may appear to be grandiose schemes but in reality, providing some electrical background knowledge is assumed, will be found well within the capabilities of an enthusiastic amateur. Returning to earth, the design of games for children (or adults) embodying external MOVING devices can have more appeal than the present crop of VDU oriented pastimes. It is probable that VDU games will begin to lose their appeal after the initial novelty has worn thin.

Transducer Interfacing

The Motorola PIA, like the majority of microprocessor I/O ports and home computers, is TTL compatible which means that the inputs must be within the range zero to 5 volts, a LOW being any voltage less than 0V4 and HIGH any voltage higher than 2V4. Unfortunately, the outside world doesn't conform to this copy two-state environment so it is necessary to convert all input "signals", whatever their origin, into the above acceptable form. The conversion, will in general, consist of two distinct operations:

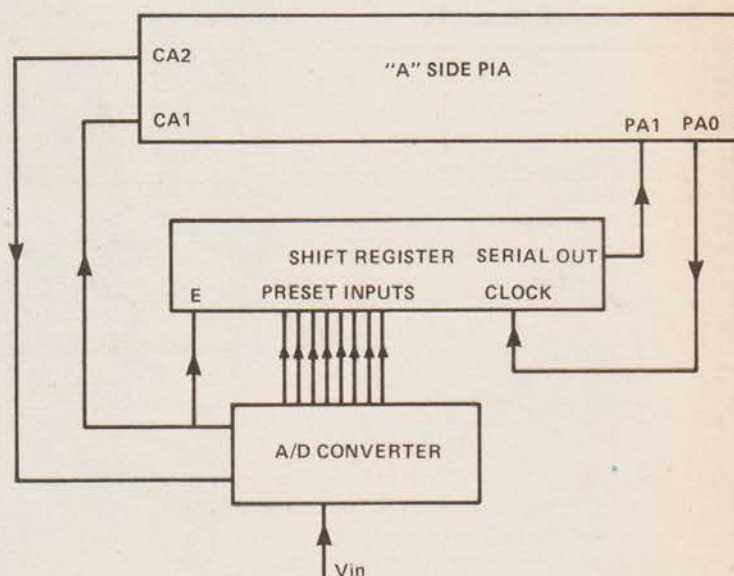
- Converting a non-electrical (physical) change into an electrical change by some form of TRANSDUCER.
- Converting the electrical output of the transducer into the right amplitude and polarity to suite TTL.

There are a host of suitable transducers on the market capable of converting almost any physical quantity into an electrical output, some examples follow:-

Photocells or photo transistors for converting light changes. Strain gauges for detecting how much something is bending (usually by stretching a resistance in the form of a tape). Thermo couples for converting temperature. Ph probes for converting degree of acidity (or alkalinity).

The electrical output of most transducers is low, probably in the millivolt or even microvolt order so the first step is to amplify (normally by an OP AMP) to bring it up to

Figure 5 Using a shift register to economise on PIA wires.



a suitable level. There is still another step however because the voltage is still an analogue of the physical quantity, ie, it is a smoothly varying voltage instead of the two-state nature acceptable to the PIA. The final component in the change is therefore some form of analogue to digital converter to change a voltage level into a binary number proportional to the level. A/D converters are in most cases "eight-bit" resolution which implies that an analogue voltage can be digitised into 2^8 (256) increments, (See Figure 4 previously).

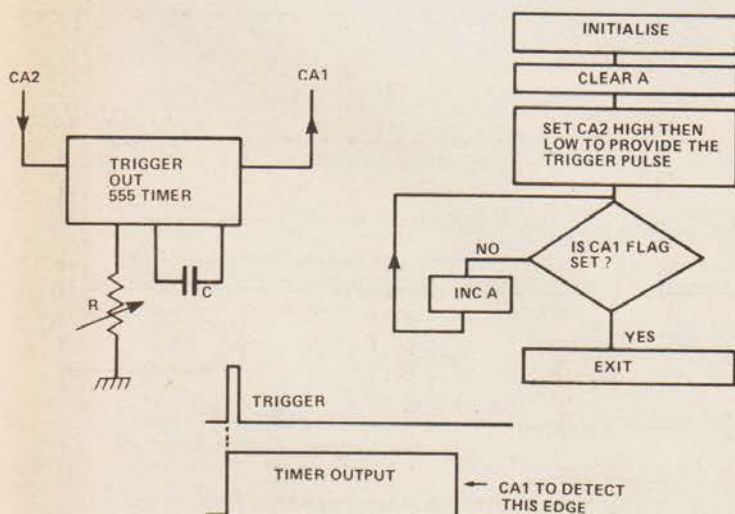
Returning to the subject of economical use of the PIA, it is clear that we must "waste" ten of the available twenty wires if we insist on the minimum amount of extra hardware to convert. Suppose we are prepared to relax a little and allow a TTL shift register between the A/D and the PIA as shown in figure 5.

The shift register has parallel inputs which are enabled-in on a pulse from the A/D data valid signal to the E pin on the register. Eight pulses from PA0 can now shift out the parallel word bit by bit into PA1. The programming of the system may take a few more bytes than the straightforward method shown earlier in Figure 4 but six PIA wires (PA2 to PA7) have been freed.

Examples Of Interfacing

The following outline systems may be found useful, if only to stimulate thought on possible projects. The flow charts indicate the software required.

Figure 6 Digitising a resistance valve.

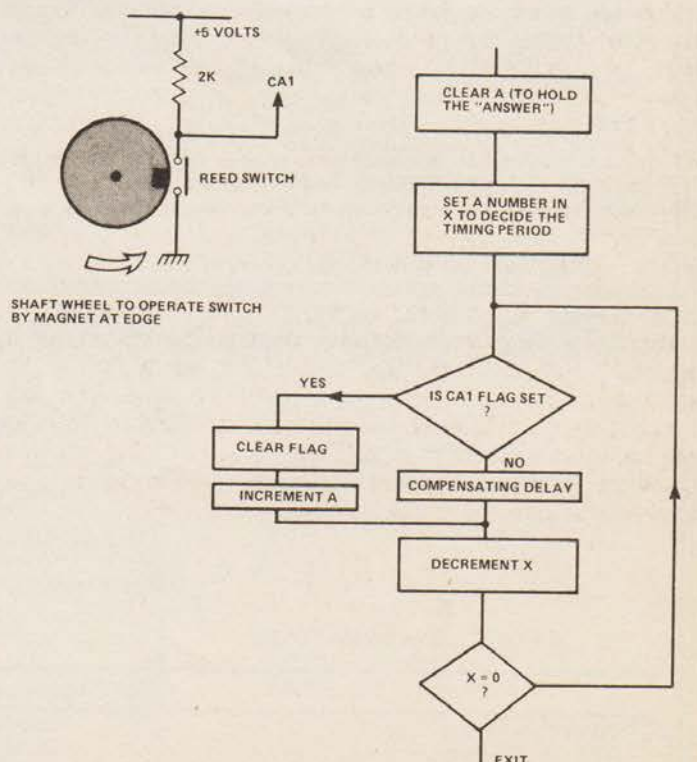


Action is quite straightforward: Timer output rests LOW and turns HIGH on the receipt of a trigger pulse. Depending on the value of R, the output eventually turns LOW again. Thus CA1 must be initialised to be ACTIVE LOW to detect this fall. The flow chart shows how the count in accumulator A will gradually increase and the final count (depending on the setting of R) will be in A when the loop exits. To allow for the restriction that R must not be allowed to fall too near zero, (by adding a fixed padder resistor) the accumulator can start with some fixed offset value instead of being cleared. Note that only two of the PIA wires have been used.

This is an example of "lateral thinking". The solution which might have immediately come to mind would probably be a tachometer geared to the shaft with the output feeding an analogue to digital converter. Apart from the expense, this solution would utilise eight I/O lines on the PIA. The method shown only uses one input (CA1) line of the PIA and although superficially crude, would be equally (if not more) accurate.

The fundamental idea is to count how many revs (how many times the flag is set) in a given time period. The actual time period depends on the number initialised in the Index register(X); this doesn't have to be one second because scaling can be arranged after Exit. The timing accuracy is good because of the crystal controlled clock in the micro-processor. The block marked "compensating delay" is a few NOPs to balance the extra time when the flow is via Clear Flag.

Figure 7 Digitising the velocity of a shaft.



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Statements					
CLEAR	DATA	DEF	DIM	END	FOR
GOTO	GOSUB	IF...GOTO	IF...THEN	INPUT	LET
NEXT	ON...GOTO	ON...GOSUB	POKE	PRINT	READ
REM	RESTORE	RETURN	STOP		

Expressions

Operators
-, +, *, /, ↑, NOT, AND, OR, >, <, <>, >=, <=, =
RANGE 10⁻³² to 10⁺³²

Functions

ABS(X)	ATN(X)	COS(X)	EXP(X)	FRE(X)	INT(X)
LOG(X)	PEEK(I)	POS(I)	RND(X)	SGN(X)	SIN(X)
SPC(I)	SQR(X)	TAB(I)	TAN(X)	USR(I)	

String Functions

ASC(X\$)	CHR\$(I)	FRE(X\$)	LEFT\$(X\$,I)	LEN(X\$)	MID\$(X\$,I,J)
					VAL(X\$)

RIGHT\$(X\$,I)

STR\$(X)

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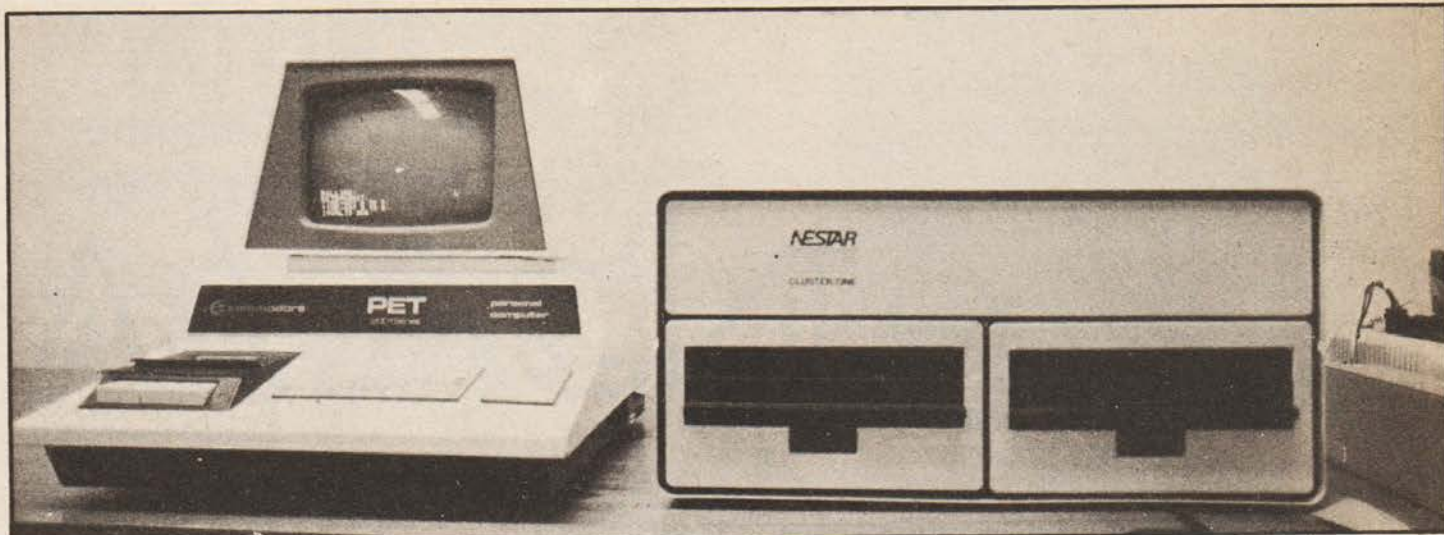
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A report from the big Apple

PETSOFT founder, Julian Allason, visited American for the National Computer Conference. From New York he sent this report:

Despite 85° heat and appalling humidity, 30,000 computerists recently made their way to the National Computer Conference, held this year in the big Apple. With over 1,700 booths spread through three locations, NCC really is the daddy of them all. Despite an ill-judged shortcut through Central Park, I survived unmugged long enough to visit all three parts of the show.

Grand Hotel?

In many ways the most interesting section was the Festival of Personal Computing, with 70 stands stuffed unceremoniously into the basement of one of New York's nastier hotels. Sadly, there was not a single British exhibitor, although a number of friendly faces were to be seen writing cheques with glazed looks.

One of the show highlights was the unveiling of the new Tandy TRS-80 Model II. This is very much a bigger brother of the Trash 80 we all know and — well, love is too strong a word. . . . Operating at twice the TRS-80's speed, the Model II is offered with either 32K or 64K of RAM and one built-in 8" floppy of half a megabyte capacity, including the Disk Operating System. U S price is \$3,450. The system can be expanded to 2 megabytes with the addition of up to three more drives.

Model II features upper and lower case letters on the 12" CRT. Format is 24 lines of 80 normal or 40 expanded characters. Level II Basic and TRSDOS operating system are resident but use up 24K of RAM. Unfortunately a number of bugs had surfaced at the last minute and it was difficult to give the system a fair assessment. The general reaction seemed to be that although it was relatively slow, Tandy's sheer marketing power would enable them to sell in quantity. February delivery was quoted for the UK, but Tandy would not be drawn on price.

Superfast Superstar

Star of the show was the Micromax Microcomputer unveiled by PET disk manufacturers Compu/Think. Featuring multiple split screen mode and 64 programmable opcodes, this looked like being a hot competitor for Tandy at around

Nestor Systems' Cluster One distributed processor: 1.3 megabyte disk unit and PET used as a controller. Photo by Julian Allason.

half the price. The Minimax uses a hybrid 6502 chip rated at 2 megahertz, which is very fast indeed. It has 106K of internal memory, and a full size IBM compatible keyboard. Double density dual drives store or retrieve up to a massive 2.4 megabytes of information at 15,000 characters per second. By my reckoning that is more information retrieved faster than any micro computer yet produced.

The split screen mode is fascinating since different parts can be used for totally different processes. Individual field editing is possible with field protect and automatic skip to the next field; another feature not previously seen on a micro computer. It also has superb high resolution graphics with 240 x 512 separately addressable dots on the 12" screen.

The consensus seemed to be that the Micromax is the most advanced microcomputer yet seen. Certainly the design approach has been to stuff as many mainframe features in as possible. Coupled with its massive storage capacity, it adds up to a pretty impressive package. US prices from \$4,495. UK availability in November.



NCC SHOW REPORT



Dr. Harry Saal, President of Nestar Systems, with his Cluster One distributed processing system. Photo: Julian Allason

Hardware, Software and Texas

Quite a wide range of printers was on show, perhaps the most interesting of which was the Comprint priced at just \$425. This prints on 8½" wide aluminium coated paper at a fast 225 characters per second. The nine by twelve matrix gives very sharp printing in both upper and lower case. Surprisingly, the results photocopy perfectly. Comprint are expected to announce UK distributors shortly.

Commodore and Apple shunned the Personal Computing Festival and were to be found over the road at

the hideously ugly 2000 bedroom Hilton skyscraper. Apple are obviously doing well since their suite was actually larger than IBM's. An interesting feature of their exhibit was the Cluster One distributed processor by Nestar Systems. Genial Harry Saal explained how it could be used to link up to 15 Apples, PETs and TRS-80's to a central 1.3 megabyte disk system. The prospect of distributed processing for \$5000 (plus the cost of each micro computer) had quite a number of mainframe men and educationalists sitting up and taking notice.

Back at the Personal Computing Festival, the emphasis seemed to be very much on software. Osborne & Associates, Speakeasy and Personal Software, all drew large crowds. The latter showed their new Visi-Calc program, which has to be one of the most sophisticated all purpose calculator programs yet developed. Software from all three companies is currently available in England from most computer stores or direct from PETSOFT. (Plug plug!)

Finally, there was news from Texas — at last! After many rumours, hints and leaks, T I finally unveiled their microcomputer. It turned out to bear a close resemblance to the Atari, which is to say that it is essentially games oriented. The other manufacturers were breathing sighs of relief. For the UK price of a projected £645, plus £400 more for an American standard TV or video output monitor, since the US protocol is incompatible with British TV's. However, I can report that T I's hospitality suite still mix the best Mint Juleps available North of the Potomac!

STOP PRESS: Late result from the great Micro Mouse Contest. (That's a micro-controlled mini robot contest through a maze) 20 to 1 outsider, Moonlight Flash, raced through the maze to claim the \$1000 prize. Trainer George Curtis of Battelle Memorial Institute told your correspondent that he was equally pleased with Moonlight Express, a large piebald mouse from the same stable who claimed the Best Learning prize. The favourite was said to have 'aborted' and stewards are to hold an enquiry into doping allegations.

Petsoft founder, Julian Allason with wife Jessica. Photo Daily Mail



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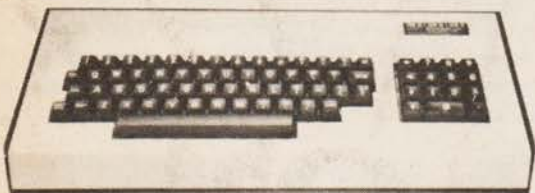
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Dateline 5000

A game to space out your evenings

This program is based partly on John Waddington's board game, '4000 AD', and partly on the popular television programme, 'Star Trek', although most of it is original. It is not so simple and corny as to be too boring, and yet at the same time, is easy to play. The object of the game is to build up as large a fleet of starships as possible, before being annihilated by the enemy. For this reason each game is different, and the length of games is enormously variable; one can try to beat one's previous record etc. The information given should adequately describe the program, but it is recommended, that, if possible the program is actually tried out.

The game is designed to run on a Texas Instruments TI-59 calculator with the PC-100C Print/Security cradle. The PC-100A or B Print cradles may be used instead.

The program is best recorded on two magnetic cards; one for the program itself, and the other to record the memories (as for printing reasons these must be entered at the start). If a different game is required each time, a random number seed between 0 and 199017 (inc) should be entered into register 9, also at the start of the game. The program should be run with the Master Library module in place (supplied with calculator), and with the partition set to 479.59 (power up partition).

The program is controlled by means of the five user-defined keys alone, using only their first functions, (A-E).

The program itself, and memory contents, are supplied as a printer listing. The game may be altered slightly by changing the names of the 12 stars. Registers 36 and 37, contain the print codes for the first star, and 58 and 59 contain those for the twelfth and last star.

Program Scenario

The game is set in the future, at a time when the United Nations have sent out a fleet of starships to colonise the worlds. Matter transportation has been perfected, and any resources found, can be immediately 'beamed' back to the home colonies, in order to build more starships. For each 'planetful', of raw materials, and each one of life-forms, providing the necessary manpower, one new starship is manufactured, during each interstellar journey, and being in possession of light-warp drive, each of these new ships, joins the main fleet before the end of the journey. The objective is therefore to colonise as many planets containing these vital resources, as possible, thereby obtaining the largest fleet possible.

However, some of these planets have already been colonised by Earth's old enemies, the Romulans and the Klingons. The UN fleet, on encountering one of these colonies, may elect to withdraw and resume the search, or to attack the settlement. If the attack is made, the battle will continue until one fleet is totally annihilated; this will be the fleet with the fewest ships (the colony will of course reply to the attack by dispatching a fleet of battle-cruisers). If both fleets are the same size, then because UN starships are slightly larger and better equipped than alien battle-cruisers, the UN fleet will win through.

The situation is further complicated by the occasional approach of the UN fleet towards the neutral zones, and statutory space of the aliens. When this happens, most of the time, the approach is uneventful; however, sometimes, the aliens, being of treacherous nature, actually cross their boundaries, and commence a spontaneous unprovoked attack on the allied fleet. In this event, the same rules of battle as previously described, apply. Although, the enemy fleets are proportioned according to the allied fleet, the greater the size of the allied fleet, the smaller the chances of its destruction (the UN fleet starts off with two ships, and all enemy fleets have *at least* two).

The greatest fleet size hitherto obtained before annihilation, was 3,130 starships (defeated by a fleet of 3,144 battle-cruisers). The least was of course, 2 starships.

Planet Identification

Planets are denoted by their Sun's name, followed by their numerical order from the Sun; ie., Earth is SOL 3.

The twelve stars used are divided into two categories, alpha-stars, and beta-stars; please see flow chart for the differences between them. The alpha stars used here, are as follows:—

ALBIREO, ACRUX, MENKAR, SOL, GEMMA & PAVO.

The beta-stars are:—

ALGOL, PROCYON, CASTOR, POLLUX, ENIF & SPICA.

Of these Procyon, Castor, Albireo, Menkar and Pavo have planets housing alien colonies at the start of the game, although these colonies readily change around during the game.

The same planet will always contain the same resources, however, throughout the game.

User Instructions

1. To start the game, first ensure the master library module is in position. Next, ensure the calculator is connected to a print cradle of the PC-100' series, and check that the partition is set to 479.59. Now, enter the program and data memories, either directly, or from each side of two magnetic cards.

Press A. (First user-defined key)

2. If destroyed in an interstellar battle with Romulan or Klingon battle-cruisers, start again. Otherwise, the printer will have written "On course for" and then a destination, eg "CASTOR 8".

If it is desired to investigate this planet, Press B. and proceed to step 3.

If it is desired to withdraw and resume search, return to stage 2 and Press C.

3. If the planet is uninhabited, parking orbit will be established, and the surface scanned by sensors. Any resources present, will automatically be utilised, and the fleet will continue on course for another planet (or alien space); go to step 2. If there is an alien colony present, then;

If it is desired to attack the colony,

Press D. and if successful, procedure will continue as if colony had not been there, ie., go to step 2.

If attack is unsuccessful, game will terminate, — if desired, Press A to start again.

If (as is the safest strategy early in the game) it is

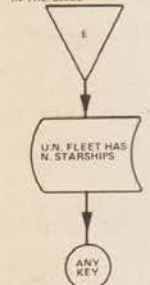
desired to withdraw from danger of enemy colony,
Press C. and go to step 2.

4. At any point in the game, E may be pressed, to print the
size of the United Nations' Fleet.

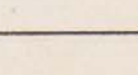
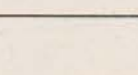
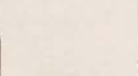
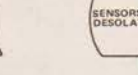
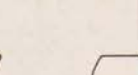
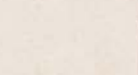
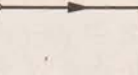
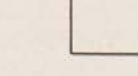
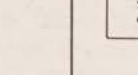
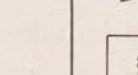
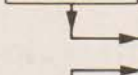
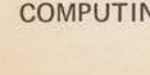
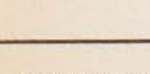
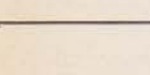
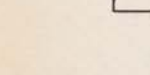
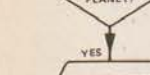
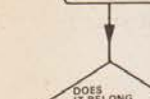
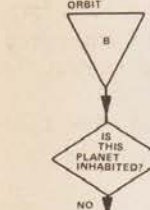
1. Simplified Flowchart for the game.

The Flow Chart should clear up any points still not
understood so far. However, please note that the chart does
not show all of the subroutines and branches in the actual
program, but is vastly oversimplified to show just the
behaviour of the program, in a reasonably comprehensible
fashion.

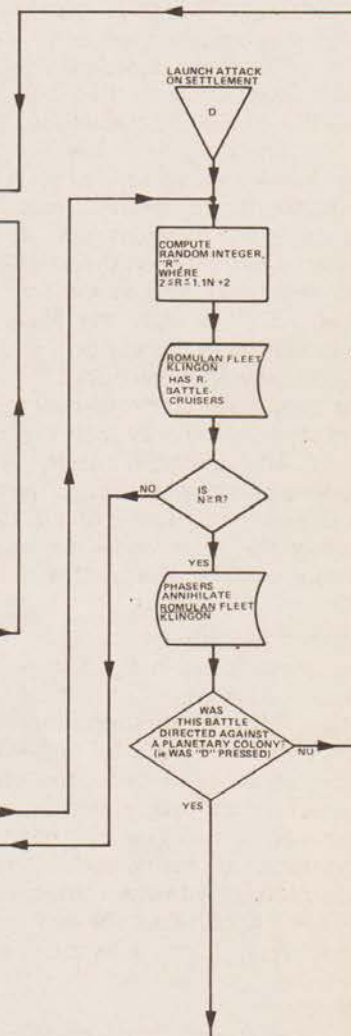
PRESSING THIS KEY IS
OPTIONAL AT ANY POINT
IN THE GAME



MOVE TOWARD
ORBIT



NOTE —
RANDOM BRANCH OUTLETS
ARE CONTROLLED BY A UNIFORMLY
DISTRIBUTED RANDOM NUMBER
GENERATOR AND THE COMPARATIVE
PROBABILITIES OF EACH OUTLET ARE
DENOTED BY A NUMBER IN PLACE OF THE
USUAL 'YES' OR 'NO' ETC.



2. Program listing for Dateline 5000.

000	76	LBL	051	68	NOP	102	06	6	154	48	RCL
001	10	E'	052	01	1	103	95	=	155	33	33
002	36	PGM	053	77	GE	104	42	STD	156	69	DP
003	15	15	054	00	00	105	02	02	157	01	01
004	71	SBR	055	69	69	106	32	XIT	158	43	RCL
005	88	DMS	056	68	NOP	107	03	3	159	34	34
006	92	RTN	057	43	RCL	108	02	2	160	69	DP
007	76	LBL	058	23	23	109	03	3	161	02	02
008	16	A'	059	48	EXC	110	01	1	162	03	3
009	69	DP	060	33	33	111	00	0	163	06	6
010	00	00	061	42	STD	112	00	0	164	03	3
011	76	LBL	062	23	23	113	69	DP	165	03	3
012	18	C'	063	43	RCL	114	00	00	166	01	1
013	42	STD	064	24	24	115	69	DP	167	03	3
014	07	07	065	48	EXC	116	01	01	168	01	1
015	73	RC*	066	34	34	117	01	1	169	05	5
016	07	07	067	42	STD	118	03	3	170	01	1
017	69	DP	068	24	24	119	42	STD	171	07	7
018	01	01	069	25	CLR	120	07	07	172	19	D'
019	69	DP	070	42	STD	121	98	ADV	173	98	ADV
020	27	27	071	36	36	122	17	B'	174	10	E'
021	76	LBL	072	43	RCL	123	05	5	175	65	X
022	17	B'	073	03	03	124	09	9	176	05	5
023	73	RC*	074	85	+	125	22	INV	177	95	=
024	07	07	075	43	RCL	126	77	GE	178	32	XIT
025	69	DP	076	04	04	127	79	X	179	01	1
026	02	02	077	95	=	128	73	RC*	180	22	INV
027	69	DP	078	55	+	129	02	02	181	77	GE
028	27	27	079	02	2	130	69	DP	182	13	C
029	73	RC*	080	95	=	131	01	01	183	69	DP
030	07	07	081	75	-	132	69	DP	184	00	00
031	76	LBL	082	53	(133	22	22	185	03	3
032	19	D'	083	24	CE	134	73	RC*	186	03	3
033	69	DP	084	75	-	135	02	02	187	42	STD
034	03	03	085	43	RCL	136	69	DP	188	07	07
035	69	DP	086	03	03	137	02	02	189	17	B'
036	05	05	087	54)	138	10	E'	190	02	2
037	25	CLR	088	50	IXI	139	65	X	191	08	8
038	92	RTN	089	95	=	140	01	1	192	16	A'
039	76	LBL	090	44	SUM	141	01	1	193	15	E
040	11	A	091	01	01	142	85	+	194	14	D
041	02	2	092	10	E'	143	02	2	195	13	C
042	42	STD	093	65	X	144	95	=	196	76	LBL
043	01	01	094	01	1	145	59	INT	197	14	D
044	15	E	095	04	4	146	42	STD	198	43	RCL
045	42	STD	096	95	=	147	36	36	199	33	33
046	03	03	097	59	INT	148	19	D'	200	69	DP
047	42	STD	098	65	X	149	98	ADV	201	01	01
048	04	04	099	02	2	150	25	CLR	202	43	RCL
049	76	LBL	100	85	+	151	91	R/S	203	34	34
050	13	C	101	03	3	152	76	LBL	204	69	DP
						153	79	X	205	02	02

206	43	RCL	258	60	DEG	310	03	3	362	00	00
207	21	21	259	43	RCL	311	03	3	363	69	DP
208	69	DP	260	20	20	312	06	6	364	27	27
209	03	03	261	19	D*	313	19	D*	365	17	B*
210	43	RCL	262	98	ADV	314	98	ADV	366	98	ADV
211	22	22	263	98	ADV	315	92	RTN	367	03	3
212	69	DP	264	98	ADV	316	76	LBL	368	06	6
213	04	04	265	98	ADV	317	22	INV	369	01	1
214	69	DP	266	91	R/S	318	69	DP	370	07	7
215	05	05	267	76	LBL	319	32	32	371	03	3
216	10	E*	268	60	DEG	320	69	DP	372	01	1
217	65	*	269	06	6	321	10	10	373	03	3
218	43	RCL	270	44	SUM	322	64	PD*	374	06	6
219	01	01	271	07	07	323	02	02	375	69	DP
220	65	*	272	17	B*	324	04	4	376	01	01
221	01	1	273	06	6	325	05	5	377	05	5
222	93	.	274	00	0	326	52	EE	378	42	STD
223	01	1	275	32	X/T	327	08	8	379	07	07
224	85	+	276	43	RCL	328	22	INV	380	17	B*
225	02	2	277	02	02	329	52	EE	381	69	DP
226	95	=	278	22	INV	330	69	DP	382	00	00
227	59	INT	279	77	GE	331	04	04	383	04	4
228	99	PRT	280	25	CLR	332	43	RCL	384	08	8
229	32	X/T	281	92	RTN	333	33	33	385	32	X/T
230	02	2	282	76	LBL	334	69	DP	386	43	RCL
231	08	8	283	15	E	335	01	01	387	02	02
232	16	A*	284	98	ADV	336	43	RCL	388	50	IXI
233	98	ADV	285	02	2	337	34	34	389	77	GE
234	01	1	286	00	0	338	69	DP	390	04	04
235	03	3	287	16	A*	339	02	02	391	06	06
236	03	3	288	43	RCL	340	43	RCL	392	08	8
237	07	7	289	01	01	341	00	00	393	32	X/T
238	01	1	290	99	PRT	342	19	D*	394	43	RCL
239	07	7	291	69	DP	343	15	E	395	36	36
240	00	0	292	00	00	344	91	R/S	396	77	GE
241	00	0	293	03	3	345	76	LBL	397	04	04
242	00	0	294	06	6	346	12	B	398	73	73
243	00	0	295	03	3	347	73	RC*	399	03	3
244	69	DP	296	07	7	348	02	02	400	01	1
245	04	04	297	01	1	349	69	DP	401	42	STD
246	02	2	298	03	3	350	32	32	402	07	07
247	05	5	299	03	3	351	29	CP	403	17	B*
248	18	C*	300	05	5	352	22	INV	404	98	ADV
249	69	DP	301	69	DP	353	77	GE	405	13	C
250	00	00	302	02	02	354	22	INV	406	43	RCL
251	43	RCL	303	03	3	355	76	LBL	407	08	08
252	21	21	304	06	6	356	25	CLR	408	69	DP
253	69	DP	305	02	2	357	98	ADV	409	01	01
254	04	04	306	03	3	358	01	1	410	43	RCL
255	43	RCL	307	02	2	359	05	5	411	35	35
256	01	01	308	04	4	360	16	A*	412	69	DP
257	77	GE	309	03	3	361	69	DP	413	02	02

414	43	RCL	431	61	GTD	448	16	A*	465	03	3
415	36	36	432	69	DP	449	76	LBL	466	01	1
416	32	XIT	433	76	LBL	450	69	DP	467	03	3
417	03	3	434	39	CDS	451	69	DP	468	07	7
418	67	EQ	435	01	1	452	00	00	469	19	D*
419	39	CDS	436	03	3	453	03	3	470	98	ADV
420	04	4	437	03	3	454	03	3	471	61	GTD
421	67	EQ	438	01	1	455	03	3	472	13	C
422	39	CDS	439	01	1	456	05	5	473	01	1
423	05	5	440	06	6	457	69	DP	474	00	0
424	67	EQ	441	19	D*	458	02	02	475	16	A*
425	39	CDS	442	69	DP	459	01	1	476	69	DP
426	68	NOP	443	23	23	460	07	7	477	24	24
427	69	DP	444	69	DP	461	03	3	478	61	GTD
428	05	05	445	24	24	462	06	6	479	69	DP
429	69	DP	446	01	1	463	01	1			
430	23	23	447	00	0	464	07	7			

DATA MEMORIES, ALSO
TO BE ENTERED AT THE
START OF THE GAME.

		2431220032.	16	-1336373235.	41
		3514243700.	17	33.	42
		1532312124.	18	3227274144.	43
		3530171600.	19	0.	44
		4140314000.	20	17312421.	45
		2127171737.	21	0.	46
		23133600.	22	3633241513.	47
		353230.	23	1327.	48
		4127133100.	24	-1424351732.	49
1532273231.	00	3323133617.	25	0.	50
0.	01	3536001331.	26	1315354144.	51
0.	02	3124232427.	27	30.	52
0.	03	1413373727.	28	-1731261335.	53
0.	04	1720153541.	29	0.	54
3235360016.	05	2436173536.	30	363227.	55
1737171537.	06	1617363227.	31	0.	56
0.	07	1337243231.	32	2217303013.	57
2724211720.	08	262724.	33	0.	58
193342.7196	09	3122323100.	34	-33134232.	59
351343.	10	2132353036.	35		
30133717.	11	0.	36		
3524132736.	12	1327223227.	37		
1532413536.	13	3335.	38		
1700213235.	14	-3215453231.	39	PARTITION - 479.59	
33133526.	15	15.	40	MODULE - MASTER 1	

3. Sample run of the program.
Letters indicate key depressed, lines show
stages of execution.

(A) —————
U.N. FLEET HAS
2.
STARSHIPS

ON COURSE FOR
GEMMA 8

(B) —————
PARKING ORBIT
CONFIRMED

SENSORS DETECT
LIFE-FORMS
PRESENT

ON COURSE FOR
ROMULAN SPACE

ON COURSE FOR
POLLUX 5

(B) —————
PARKING ORBIT
CONFIRMED

SENSORS DETECT
DESOLATION

ON COURSE FOR
ALGOL 7

(B) —————
PARKING ORBIT
CONFIRMED

SENSORS DETECT
RAW MATERIALS
PRESENT

ON COURSE FOR
MENKAR 1

(C) —————
ON COURSE FOR
ROMULAN SPACE

ON COURSE FOR
PAYD 2

(C) —————
ON COURSE FOR
ROMULAN SPACE

ON COURSE FOR
KLINGON SPACE

KLINGON
BATTLE-CRUISERS

U.N. FLEET HAS
7.
STARSHIPS

KLINGON FLEET HAS
4.
BATTLE-CRUISERS

PHASERS ANNIHILATE
KLINGON FLEET

ON COURSE FOR
ACRUX 7

(C) —————
ON COURSE FOR
ALBIRED 7

(C) —————
ON COURSE FOR
ENIF 4

(B) —————
PARKING ORBIT
CONFIRMED

SENSORS DETECT
DESOLATION

ON COURSE FOR
MENKAR 4

(B) —————
KLINGON COLONY

U.N. FLEET HAS
11.
STARSHIPS

(D) —————
KLINGON FLEET HAS
5.
BATTLE-CRUISERS

PHASERS ANNIHILATE
KLINGON FLEET

PARKING ORBIT
CONFIRMED

SENSORS DETECT
LIFE-FORMS AND
RAW MATERIALS
PRESENT

ON COURSE FOR
ALGOL 8

(C) —————
ON COURSE FOR
KLINGON SPACE

ON COURSE FOR
ALBIRED 9

(B) —————
ROMULAN COLONY

U.N. FLEET HAS
17.
STARSHIPS

(D) —————
ROMULAN FLEET HAS
18.
BATTLE-CRUISERS

PHASERS ANNIHILATE
U.N. FLEET

The program has been written for the Triton in 2½K and will print a monthly calender corrected for leap years up to the end of the century.

The Year 2000 will not be a leap year and a simple alteration will allow the program to run to the 21st century. The program will output to the printer under the Humbug monitor (statement 45) and this can be deleted to give VDU output. A sample run is given for May to September 1979.

```

5  V=12;F00A=10000;JLYTA
13  A=3;B=0;C=0;D=2;E=0;F=0;G=0;H=0;I=0;J=0;K=0;L=0;M=0
23  PRINT'80TH CENTURY CANDLEMAD'
33  INPUT'ENTER THE NUMBER OF THE MONTH YOU REQUIRE'D
31  IF<PRINT'INVALID ENTRY';GOTO33
32  IF>12PRINT'INVALID ENTRY';GOTO33
40  INPUT'ENTER THE YEAR YOU REQUIRE'D
41  IF<1979PRINT'YEAR ENTERED MUST BE 1979 OR LATER';GOTO40
45  DOBLE522;2170;PRINT
46  PRINT'CALLIDAP FOR MONTH',#3,D,*****
47  PRINT'FOR THE YEAR',#3,C
48  PRINT
50  Y=1979
60  T=3
75  Y=0
80  A=1
100  F00A=AT0A+30
105  V=1
110  B=B+1
120  IFB>7LETB=B-7
175  IFQ=730SUB3300
200  JLYTA;30SUB5000
210  T=A-1
260  IFY=130T0270
265  IFY=130T0330
270  Y=Y+1
271  F00A=AT0A+28
275  B=B+1
280  IFB>7LETB=B-7
287  IFQ=730SUB3300
290  JLYTA;30SUB5000
295  T=A-1;30T0500
300  Y=Y+1
305  F00A=AT0A+27
310  B=B+1
320  IFB>7LETB=B-7
375  IFQ=730SUB3300
400  JLYTA;30SUB5000
410  T=A-1
500  Y=Y+1
505  F00A=AT0A+30
510  B=B+1
520  IFB>7LETB=B-7
575  IFQ=730SUB3300
600  JLYTA;30SUB5000
610  T=A-1
700  Y=Y+1
705  F00A=AT0A+29
710  B=B+1
720  IFB>7LETB=B-7
775  IFQ=730SUB3300
800  JLYTA;30SUB5000
810  T=A-1
900  Y=Y+1
905  F00A=AT0A+30
910  B=B+1
920  IFB>7LETB=B-7
975  IFQ=730SUB3300
1000  JLYTA;30SUB5000
1010  T=A-1
1130  Y=Y+1
1135  F00A=AT0A+29
1140  B=B+1
1150  IFB>7LETB=B-7
1175  IFQ=730SUB3300
1200  JLYTA;30SUB5000
1210  T=A-1
1300  Y=Y+1
1335  F00A=AT0A+30
1340  B=B+1
1350  IFB>7LETB=B-7
1375  IFQ=730SUB3300
1400  JLYTA;30SUB5000
1410  T=A-1
1500  Y=Y+1
1535  F00A=AT0A+30
1540  B=B+1
1550  IFB>7LETB=B-7
1575  IFQ=730SUB3300
1600  JLYTA;30SUB5000
1610  T=A-1
1700  Y=Y+1
1735  F00A=AT0A+29
1740  B=B+1
1750  IFB>7LETB=B-7
1775  IFQ=730SUB3300
1800  JLYTA;30SUB5000
1810  T=A-1
1900  Y=Y+1
1935  F00A=AT0A+30
1940  B=B+1
1950  IFB>7LETB=B-7
1975  IFQ=730SUB3300
2000  JLYTA;30SUB5000
2010  T=A-1
2100  Y=Y+1
2135  F00A=AT0A+29
2140  B=B+1
2150  IFB>7LETB=B-7
2175  IFQ=730SUB3300
2200  JLYTA;30SUB5000
2210  T=A-1
2300  Y=Y+1
2335  F00A=AT0A+30
2340  B=B+1
2350  IFB>7LETB=B-7
2375  IFQ=730SUB3300
2400  JLYTA;30SUB5000
2410  T=A-1
2475  LETY=Y+1
2480  LETY=Y+1
2435  IFY=5LETY=Y-4
2500  GOTO100
3000  IFY#7GOTO4000
3100  IFB=1PRINT' MON',#3,A-T,,,
3200  IFB=2PRINT' TUE',#3,A-T,,,
3300  IFB=3PRINT' WED',#3,A-T,,,
3400  IFB=4PRINT' THU',#3,A-T,,,
3500  IFB=5PRINT' FRI',#3,A-T,,,
3600  IFB=6PRINT' SAT',#3,A-T,,,

```

```

3780 IFB=7PRINT' SUN'##3,1-T,,,
3800 IFA-T=7PRINT
3810 IFA-T=14PRINT
3820 IFA-T=21PRINT
3830 IFA-T=28PRINT
4000 RETURN
5000 IFI=010T06000
5500 RETURN
6000 IFI=010T03000
7000 RETURN
8000 PRINT
8250 PRINT' END OF MONTH'##3,0,.....
8500 IFY=1PRINT' FOR THE LEAD-YEAR',0
8600 IFY=1PRINT' FOR THE YEAR',0
8750 PRINT
8900 PRINT' REMINDERS.....'
9010 PRINT
9020 PRINT
9050 POKLS123,22216
9500 GOTO5

```

A specimen run for May – September 1979.

```

CALENDAR FOR MONTH 5                      FOR THE YEAR 1979
TUE 1  WED 2  THU 3  FRI 4  SAT 5  SUN 6  MON 7
TUE 8  WED 9  THU 10  FRI 11  SAT 12  SUN 13  MON 14
TUE 15  WED 16  THU 17  FRI 18  SAT 19  SUN 20  MON 21
TUE 22  WED 23  THU 24  FRI 25  SAT 26  SUN 27  MON 28
TUE 29  WED 30  THU 31
END OF MONTH 5                      FOR THE YEAR 1979

```

REMINDEES.....

```

CALENDAR FOR MONTH 6                      FOR THE YEAR 1979
FRI 1  SAT 2  SUN 3  MON 4  TUE 5  WED 6  THU 7
FRI 8  SAT 9  SUN 10  MON 11  TUE 12  WED 13  THU 14
FRI 15  SAT 16  SUN 17  MON 18  TUE 19  WED 20  THU 21
FRI 22  SAT 23  SUN 24  MON 25  TUE 26  WED 27  THU 28
FRI 29  SAT 30
END OF MONTH 6                      FOR THE YEAR 1979

```

REMINDEES.....

```

CALENDAR FOR MONTH 7                      FOR THE YEAR 1979
SUN 1  MON 2  TUE 3  WED 4  THU 5  FRI 6  SAT 7
SUN 8  MON 9  TUE 10  WED 11  THU 12  FRI 13  SAT 14
SUN 15  MON 16  TUE 17  WED 18  THU 19  FRI 20  SAT 21
SUN 22  MON 23  TUE 24  WED 25  THU 26  FRI 27  SAT 28
SUN 29  MON 30  TUE 31
END OF MONTH 7                      FOR THE YEAR 1979

```

REMINDEES.....

```

CALENDAR FOR MONTH 8                      FOR THE YEAR 1979
WED 1  THU 2  FRI 3  SAT 4  SUN 5  MON 6  TUE 7
WED 8  THU 9  FRI 10  SAT 11  SUN 12  MON 13  TUE 14
WED 15  THU 16  FRI 17  SAT 18  SUN 19  MON 20  TUE 21
WED 22  THU 23  FRI 24  SAT 25  SUN 26  MON 27  TUE 28
WED 29  THU 30  FRI 31
END OF MONTH 8                      FOR THE YEAR 1979

```

REMINDEES.....

```

CALENDAR FOR MONTH 9                      FOR THE YEAR 1979
SAT 1  SUN 2  MON 3  TUE 4  WED 5  THU 6  FRI 7
SAT 8  SUN 9  MON 10  TUE 11  WED 12  THU 13  FRI 14
SAT 15  SUN 16  MON 17  TUE 18  WED 19  THU 20  FRI 21
SAT 22  SUN 23  MON 24  TUE 25  WED 26  THU 27  FRI 28
SAT 29  SUN 30
END OF MONTH 9                      FOR THE YEAR 1979

```

REMINDEES.....



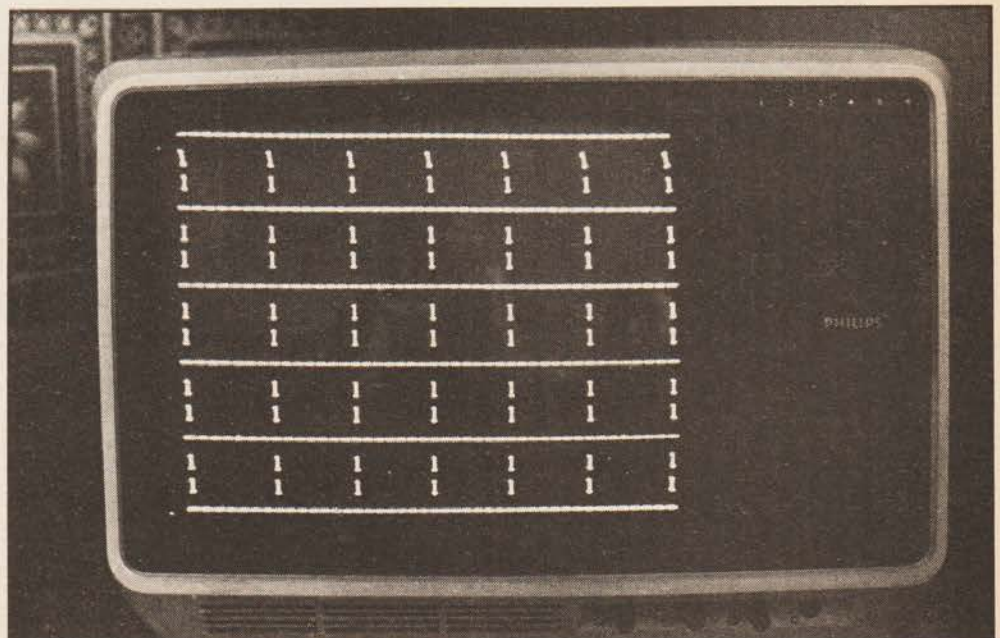
Check out your CRT

One of the biggest problems with colour television sets, before the advent of the 20AX tube, is the adjustment of the convergence of the three colour guns. When these adjustments are in need of attention the picture becomes blurred and colour fringing takes place (eg coloured lines around the edges of faces). This can best be seen with the test card where the horizontal and vertical lines are not black but are fringed by red, green or blue.

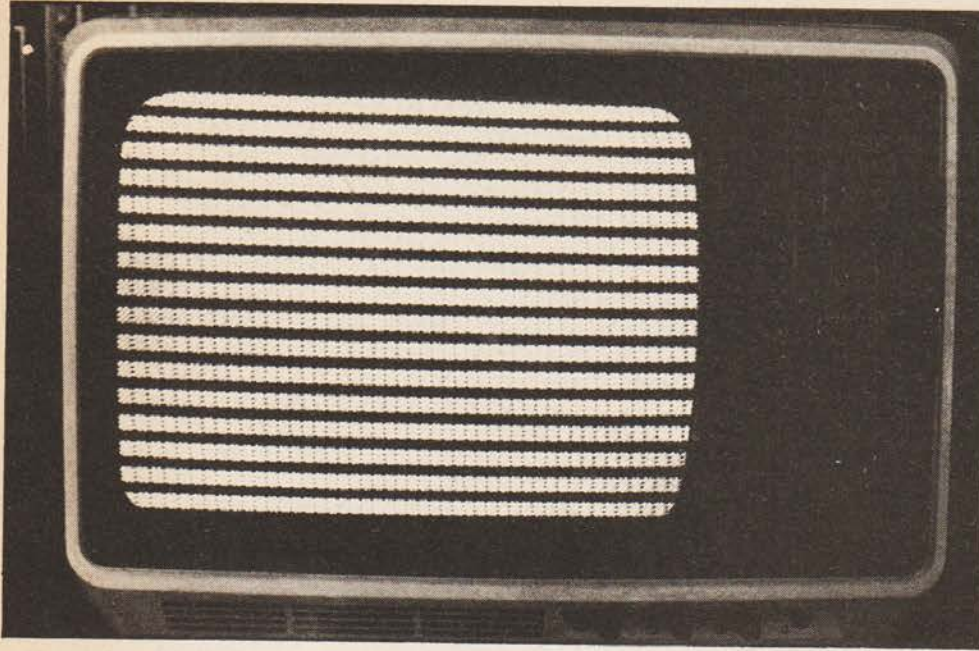
The Hardware

There are two problems associated with convergence adjustment.

1. There are approx a dozen preset resistors on the convergence panel in the back of the set. These are interactive and therefore adjustment is a question of trial and error together with a compromise in the various adjustments. Most TV sets give a *pictorial* representation of the purpose of each preset alongside.



NASCOM TELE-TEST



2. Whenever you want to make adjustments, the test card is seldom broadcast. There is nothing more infuriating than getting three pictures, one red, one green and one blue and then losing the test card for Playschool etc. Here your microprocessor can help.

Because the NASCOM 1 plugs directly into the aerial socket of the TV a test picture can be provided at will. Ah! you may say, my NASCOM is Black & White. Good comes the reply, convergence adjustments are always carried out on a black and white picture.

The Program

The program is entered at location OC60, when an index is displayed on the screen, listing the four patterns available:—

1. Purity
2. Static Convergence
3. Dynamic Convergence
4. Focus

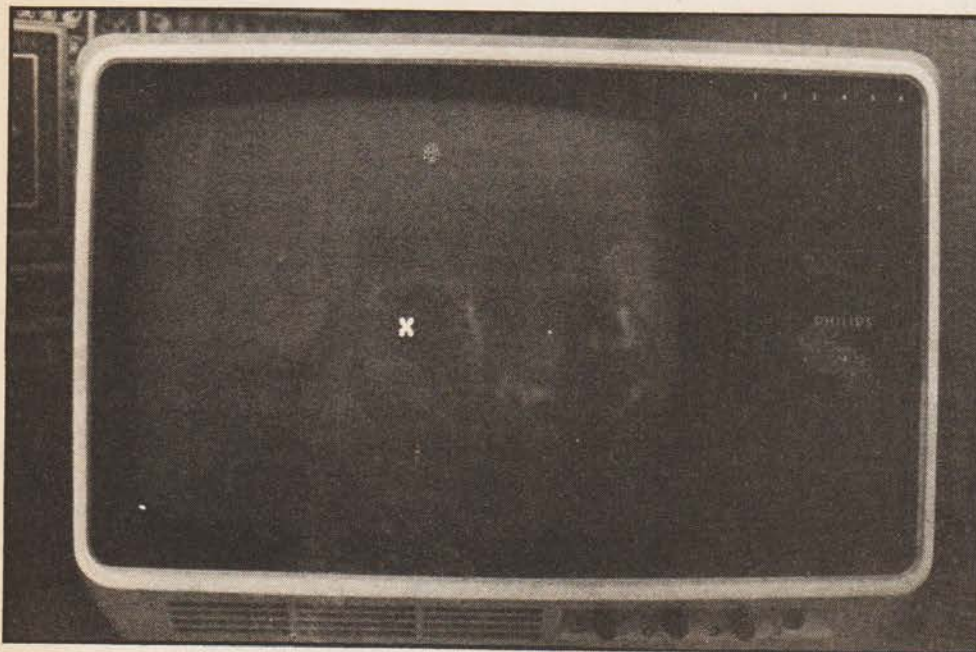
1. Purity:— This seldom needs attention. The pattern is in the form of lines of 'rub out' symbol. By switching off two colours at a time the remaining colour can be adjusted so the intensity of colour is constant over the whole screen.

2. Static Convergence:— Here an 'X' is displayed in the centre of the screen and each static magnet should be adjusted to get proper convergence of the 3 colours.

3. Dynamic Convergence:— This pattern displays a 'grid' and the various adjustments made to get the best alignment. This procedure is very much trial and error, however I would advise reading the service data for each particular set.

4. Focus:— The focus is easily set for optimum with the display of the character set distributed over the screen.

After each test has been used the index can be returned to by pressing the space bar.



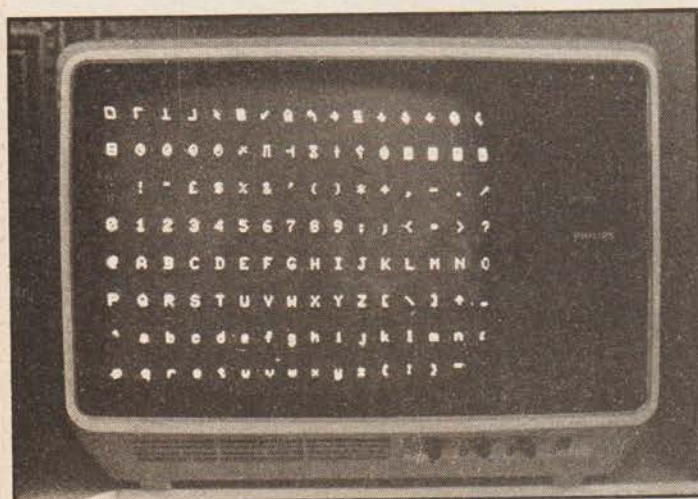
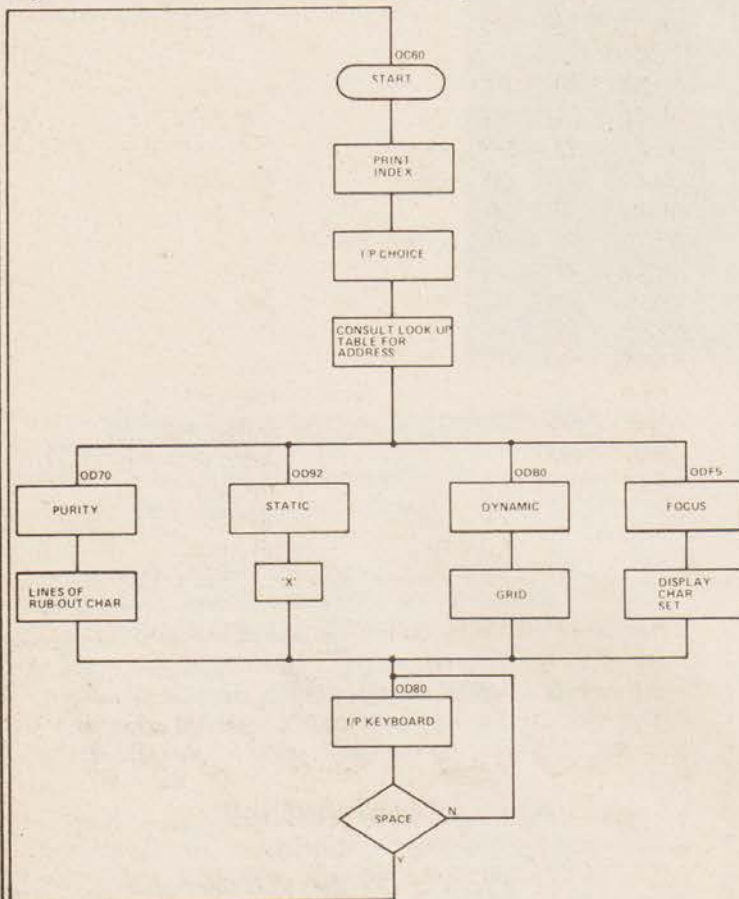
The pictures show the menu page for test selection and the four different tests possible with the program. Clockwise round the page they are Purity. Static convergence and Dynamic convergence. Focus is shown on the next page.

TELE TEST

This program will print an index and then display one of the four chosen patterns. These patterns are designed to assist in the alignment of a colour television picture.

NOTE: When entering text "/" indicates a space, and "@" indicates a new line. Execute from 0C60.

Figure 1. The flowchart for the Tele Test program.



```

0C60 EF RST 40
0C61 1E clear screen
0C62 /TELE/TEST@@@
0C6F /LIST/OF/TESTS:@@
0C81 /1///PURITY@
0C8D /2///STATIC/CONVERGENCE@
0CA5 /3///DYNAMIC/CONVERGENCE@
0CBE /4///FOCUS@@
0CCA ///WHICH/TEST/WOULD/YOU/LIKE?@@
0CE9 00 stop bit, end of string
0CEA CD 3E 00 'TT1' CALL 'CHIN' get entry
0CED FE 31 CP = 31
0CEF 38 F9 JRC 'TT1'
0CF1 FE 35 CP = 35
0CF3 30 F5 JRNC 'TT1'
0CF5 26 0D H = 0D
0CF7 6F L, A
0CF8 6E L, (HL)
0CF9 EF 1E 00 clear screen
0CFC E9 JP, (HL)

LOOK-UP TABLE
0D31 70 purity
0D32 92 static convergence
0D33 B0 dynamic convergence
0D34 F5 focus

PURITY
0D70 11 FF 07 DE = 07FF
0D73 0E 10 C = 10H
0D75 06 40 B = 40H
0D77 3E 7F A = 7F
0D79 12 (DE), A
0D7A 13 INC DE
0D7B 10 FA DJNZ -4
0D7D 0D DEC C
0D7E 20 F5 JRNZ -5
0D80 CD 3E 00 'RST' Call CHIN
0D83 3E 20 A = 20
0D85 06 40 B = 40
0D87 12 (DE), A
0D88 1B DEC DE
0D89 10 FC DJNZ -2
0D8B CD 40 02 Call CRLF
0D8E C3 60 0C JP START

STATIC CONVERGENCE
0D92 3E 1E A = 1E
0D94 CD 3B 01 Call CRT
0D97 3E 58 A = 58
0D99 32 E0 09 (09E0), A
0D9C CD 3E 00 Call CHIN
0D9F C3 60 0C JP START

DYNAMIC CONVERGENCE
Subroutine 'PRINT'
0DAB 12 (DE), A
0DAC 13 INC DE
0DAD 10 FC RET
0DAD 10 FC DJNZ -2
0DAF C9 RET

Main Prog
0DB0 11 0C 08 DE = 080D
0DB3 D9 EXX
0DB4 0E 05 C' = 5
  
```

NASCOM TELE-TEST

0DB6	06	02		B' = 2	0DE3	14		INC D
0DB8	D9			EXX	0DE4	5F		E, A
0DB9	0E	06		C = 6	0DE5	D9		EXX
0DBB	3E	6C		A = 6C	0DE6	0D		DEC C'
0DBD	12			(DE), A	0DE7	20	CD	JRNZ -49
0DBE	13			INC DE	0DE9	D9		EXX
0DBF	06	06		B = 6	0DEA	3E	2D	A = 2D
0DC1	3E	20		A = 20	0DEC	06	2B	B = 2B
0DC3	CD	AB	0D	Call PRINT	0DEE	CD	AB 0D	Call PRINT
0DC6	0D			DEC C	0DF1	18	8D	JR 'RST'
0DC7	20	F2		JRNZ -12	FOCUS			
0DC9	3E	6C		A = 6C	0DF5	3E	1E	A = 1E
0DCB	12			(DE), A	0DF7	CD	3B 01	Call CRT
0DCC	3E	16		A = 16	0DFA	11	50 00	DE = 0050
0DCE	83			add E	0DFD	21	0B 08	HL = 080B
0DCF	30	01		JRNC +3	0E00	3E	00	A = 00
0DD1	14			INC D	0E02	06	10	'LINE' B = 10
0DD2	5F			E, A	0E04	77		(HL), A
0DD3	D9			EXX	0E05	3C		INC A
0DD4	10	E2		DJNZ -28	0E06	23		INC HL
0DD6	D9			EXX	0E07	23		INC HL
0DD7	06	2B		B = 2B	0E08	23		INC HL
0DD9	3E	2D		A = 2D	0E09	10	F9	DJNZ -5
0ddb	CD	AB	0D	Call PRINT	0E0B	19		ADD HL, DE
0DDE	3E	15		A = 15	0E0C	FE	80	CP 80
0DE0	83			ADD E	0E0E	20	F2	JRNZ -12
0DE1	30	01		JRNC +1	0E10	C3	80 0D	JP 0D80

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This program is written in TRS-80 level II Basic. It occupies approximately 2.4 K bytes and should be located near the top of available RAM if it is entered in hexadecimal format. The program is simplicity itself and is really intended as a guide for those TRS-80 users who are 'still finding their way' with their equipment. It has also been written to exclude the use of Peripherals and may be run on the basic TRS-80, which includes Keyboard and VDU. However, it may easily be adapted for Line Printer use by changing the relevant PRINT statements to LPRINT.

The TRS-80 uses the Z80 Microprocessor as its CPU, hence the inclusion of a hexadecimal listing of the program for those readers who do not possess the TRS-80, but whose equipment includes the Z80 CPU; in which case the program, as listed, should operate with little or no alteration.

THE PROGRAM

The Mini Ledger program has been dimensioned for a maximum of 30 entries (the example shows 6 only), these dimensioned arrays may be reduced or increased as required the only constraint being the amount of RAM the user has available. It is important to remember that the value of N in line 170 must be equal to the number of DATA entries in lines 400 - 600. The amount of usable memory can be further conserved by deleting all REM statements once these are found to be no longer necessary.

The program is self prompting and no further explanation is considered necessary. As it stands it may not suit all requirements an intended user may need, but it is a program that can be easily altered to suit individual tasks. The PRINT USING statements, may for example, be re-arranged in a different order - or re-worded as necessary. The program need not be used as a ledger, with a little thought it could be used for many different purposes; Household accounts, Cheque-book balancing, etc., food for thought!

```

100 PRINT:CLS:PRINT
110 PRINT:INPUT"ENTER TODAY'S DATE
";D$
120 PRINT:INPUT"ENTER CREDIT CARRIED
FORWARD ";
130 PRINT"WHEN PROMPTED ENTER THE
VAT RATE IN DECIMAL"
140 PRINT"FORMAT. E.G. 0.08 FOR
8% 0.125 FOR 12.5% ETC."
150 PRINT:INPUT"ENTER VAT RATE FOR
TRANSACTIONS THIS PERIOD ";V
160 PRINT:CLS:PRINT
170 N = 6
180 REM THE ABOVE N MUST EQUAL THE
NUMBER OF DATA STATEMENTS
190 REM IN LINES 400 - 600
200 REM L = LEDGER ENTRY
NUMBER
210 REM D$ = DATE OF LEDGER
ENTRY
220 REM C = CREDITS (SALES ETC.)
230 REM D = DEBITS (PAYMENTS OUT,
ETC.)
240 REM E$ = TRANSACTION DETAILS
250 REM DELETE ALL 'REM' STATEMENTS
WHEN FAMILIARISATION OF
260 REM PROGRAM IS COMPLETE.
270 DIM L(30),D$(30),C(30),D(30),
E$(30)
280 REM REDUCE OR INCREASE THE
MAGNITUDE OF THE DIM STATEMENTS
290 REM TO SUIT RAM MEMORY AVAILABLE
YOUR SYSTEM
300 PRINT"          TODAY'S DATE
";D$
310 PRINT"  M I N I L E D G E R
P R O G R A M  "
320 PRINT"          "
330 PRINT
340 PRINT TAB(0)"LGR";TAB(7)"ENTRY";
TAB(17)"CREDITS";TAB(29)"DEBITS";

```

```

TAB(40)"TRANSACTION"
350 PRINT TAB(0)"NO.";TAB(7)"DATE";
TAB(17)"(SALES)";TAB(29)"
OUTGOING";TAB(40)"DETAILS"
360 FOR U = 0 TO 63
370 PRINT TAB(U)"-";
380 NEXT U : PRINT
400 DATA 200,"04/01/79",1229.75,0.00,
"SALES"
420 DATA 201,"04/02/79",1534.90,128.68
"SALES / GAS ACC."
430 DATA 202,"04/03/79",1675.53,3.95,
"SALES / POSTAGE"
440 DATA 203,"04/04/79",1476.24,68.98,
"SALES / TELEPHONE ACC."
450 DATA 204,"04/05/79",2995.75,1212.78,
"SALES / NEW STOCK"
460 DATA 205,"04/06/79",3114.16,124.18,
"SALES / ELECTRIC ACC."
610 Z1 = 0 : Z2 = 0 : Z3 = 0
620 FOR I = 1 TO N
630 READ L(I),D$(I),C(I),D(I),E$(I)
640 PRINT TAB(0);L(I);TAB(7);D$(I);
TAB(17);C(I);TAB(29);D(I);TAB
(40);E$(I)
650 Z1 = Z1 + C(I)
660 Z2 = Z2 + D(I)
670 Z3 = Z3 + (C(I) - C(I) * V)
680 NEXT I : RESTORE
690 FOR U = 0 TO 63
700 PRINT TAB(U)"-";
710 NEXT U : PRINT
720 PRINT USING"TOTAL DEBITS THIS
PERIOD = #####.## ";Z2
730 PRINT USING"TOTAL CREDITS THIS
PERIOD = #####.## ";Z1
740 PRINT USING"TOTAL VAT ON SALES
THIS PERIOD #####.## "Z1 * V
750 PRINT USING"TOTAL NET CREDIT
(LESS VAT) = #####.## ";Z3
760 PRINT USING"CREDIT BALANCE
BROUGHT FORWARD #####.## ";P
770 PRINT USING"CREDITS (LESS ABOVE
DEBITS) C/F ----- ";P + Z3-Z2
780 FOR U = 0 TO 63
790 PRINT TAB(U)"=";
800 NEXT U : PRINT
999 END

```

CREDIT CARRIED FORWARD = 1216.53

VAT RATE ENTERED AS 0.08 (8%)

TODAY'S DATE 05/27/79

MINI LEDGER PROGRAM

LGR No.	ENTRY DATE	CREDITS (SALES)	DEBITS OUTGOING	TRANSACTION DETAILS
200	04/01/79	1229.75	0	SALES
201	04/02/79	1534.9	128.68	SALES / GAS ACC.
202	04/03/79	1675.53	3.95	SALES / POSTAGE
203	04/04/79	1476.24	68.98	SALES / TELEPHONE ACC.
204	04/05/79	2995.75	1212.78	SALES / NEW STOCK
205	04/06/79	3114.16	124.18	SALES / ELECTRIC ACC.

TOTAL DEBITS THIS PERIOD = 1538.57
TOTAL CREDITS THIS PERIOD = 12026.30
TOTAL VAT ON SALES THIS PERIOD = 962.11
NET CREDIT (LESS VAT) = 11064.20
CREDIT BALANCE BROUGHT FORWARD = 1216.53
CREDITS (LESS ABOVE DEBITS) C/F = 10742.20

MINI LEDGER

FILESPEC: LEDGER

SECTOR: 1

```

0  35 04 66 04 60 52 3A 84 3A B2 00 EF 68 14 00 B2
28 3A 89 22 45 4E 54 45 52 20 54 4F 44 41 59 27 53
32 20 44 41 54 45 20 20 40 40 2F 44 44 2F 59 59 29
48 22 3F 44 54 24 00 17 69 1E 00 B2 3A 89 22 45 4E
64 54 45 52 20 43 52 45 44 49 54 20 43 41 52 52 49
80 45 44 20 46 4F 52 57 41 52 44 22 38 50 00 40 69
96 20 00 84 3A B2 22 57 48 45 4E 20 50 52 4F 40 50
112 54 45 44 20 45 4E 54 45 52 20 54 48 45 20 56 41
128 54 20 52 41 54 45 20 49 4E 20 44 45 43 49 40 41
144 40 22 00 35 69 32 00 B2 22 46 4F 52 40 41 54 2E
160 20 20 45 2E 47 2E 20 20 30 2E 30 38 20 46 4F 52
176 20 38 25 20 20 30 2E 31 32 35 20 46 4F 52 20 31
192 32 2E 35 25 20 20 45 54 43 2E 22 00 80 69 30 00
208 82 3A 89 22 45 4E 54 45 52 20 56 41 54 20 52 41
224 54 45 20 46 4F 52 20 54 52 41 4E 53 41 43 54 49
240 4F 4E 53 20 54 48 49 53 20 50 45 52 49 4F 44 22

```

FILESPEC: LEDGER

SECTOR: 2

```

0  38 56 00 06 69 46 00 B2 3A 84 3A B2 00 00 69 50
16 00 4E 20 05 20 36 00 00 6A 5A 00 93 20 54 48 45
32 20 41 42 4F 56 45 20 4E 20 40 55 53 54 20 45 51
48 55 41 40 20 54 48 45 20 4E 55 40 42 45 52 20 4F
64 46 20 44 41 54 41 20 53 54 41 54 45 40 45 4E 54
80 53 00 24 6A 64 00 93 20 49 4E 20 40 49 4E 45 53
96 20 34 30 30 20 20 20 36 30 30 00 48 6A 6E 00 93
112 20 20 20 20 40 20 20 20 20 20 20 30 20 20 40 45
128 44 47 45 52 20 45 4E 54 52 59 20 4E 55 40 42 45
144 52 00 73 6A 70 00 93 20 20 20 20 44 24 20 20 20
160 20 20 20 20 20 44 41 54 45 20 4F 46 20 40 45 44
176 47 45 52 20 45 4E 54 52 59 00 90 6A 02 00 93 20
192 20 20 20 43 20 20 20 20 20 20 30 20 20 43 52 45
208 44 49 54 53 20 20 20 20 53 41 40 45 53 20 45 54
224 43 2E 29 00 CF 6A 80 00 93 20 20 20 20 44 20 20
240 20 20 20 20 30 20 20 44 45 42 49 54 53 20 20 20

```

FILESPEC: LEDGER

SECTOR: 3

```

0  20 20 50 41 59 40 45 4E 54 53 20 4F 55 54 20 20
16 45 54 43 2E 29 00 F6 6A 96 00 93 20 20 20 20 45
32 24 20 20 20 20 20 30 20 20 54 52 41 4E 53 41 43
48 54 49 4F 4E 20 44 45 54 41 49 40 53 00 2F 68 00
64 00 93 20 44 45 40 45 54 45 20 41 40 40 20 27 52
80 45 40 22 20 53 54 41 54 45 40 45 4E 54 53 20 57
96 48 45 4E 20 46 41 40 49 40 49 41 52 49 53 54 49
112 4F 4E 20 4F 46 00 4A 68 0A 00 93 20 50 52 4F 47
128 52 41 40 20 49 53 20 43 4F 40 50 40 45 54 45 2E
144 00 70 6B B4 00 0A 20 40 20 33 30 29 20 44 24 28
160 33 30 29 20 43 28 33 30 29 20 44 28 33 30 29 20
176 45 24 28 33 30 29 00 00 6B BE 00 93 20 52 45 44
192 55 43 45 20 4F 52 20 49 4E 43 52 45 41 53 45 20

```

```

208 54 48 45 20 40 41 47 4E 49 54 55 44 45 20 4F 46
224 20 54 48 45 20 44 49 40 20 53 54 41 54 45 40 45
240 4E 54 53 00 00 6B 08 00 93 20 54 4F 20 53 55 49

```

FILESPEC: LEDGER

SECTOR: 4

```

0  54 20 52 41 40 20 40 45 40 4F 52 59 20 41 56 41
16 49 40 41 42 40 45 20 59 4F 55 52 20 53 59 53 54
32 45 40 2E 00 15 60 D2 00 52 22 20 20 20 20 20 20
48 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
64 20 20 20 20 20 20 20 20 20 54 4F 44 41 59 27 53
80 20 44 41 54 45 20 22 38 44 54 24 00 48 60 DC 00
96 82 22 20 20 20 40 20 49 20 4E 20 49 20 20 20 40
112 20 45 20 44 20 47 20 45 20 52 20 20 20 50 20 52
128 20 4F 20 47 20 52 20 41 20 40 20 20 20 22 00 78
144 60 F0 00 B2 22 20 20 20 20 20 20 20 20 20 20 20
160 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
176 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
192 22 00 01 60 FA 00 B2 00 08 60 04 01 B2 20 00 30
208 29 22 40 47 52 22 38 B0 37 29 22 45 4E 54 52 59
224 22 36 B0 31 37 29 22 43 52 45 44 49 54 53 22 38
240 8C 32 29 29 22 44 43 42 49 54 53 20 38 B0 34 30

```

FILESPEC: LEDGER

SECTOR: 5

```

0  28 22 54 52 41 4E 52 41 42 54 49 4F 4E 22 00 00
16 60 8E 01 62 20 B0 30 23 22 4E 6F 2E 22 38 B0 37
32 29 22 44 41 54 45 22 38 B0 31 37 29 22 20 52 41
48 40 45 53 29 22 38 B0 32 39 29 32 4F 55 54 47 4F
64 49 4E 47 22 38 B0 34 32 29 22 44 45 54 41 49 40
80 53 22 00 10 60 19 01 81 20 55 20 05 20 20 20 80
96 20 38 33 00 20 60 22 01 20 20 B2 20 B0 55 29 22
112 20 22 38 00 35 60 20 01 87 20 55 00 38 60 36 01
128 B0 00 65 60 90 01 88 20 32 30 30 20 22 30 34 2F
144 30 31 2F 37 39 22 20 31 32 32 39 2E 37 35 20 30
160 2E 20 30 20 22 53 41 40 45 53 22 00 90 60 A4 01
176 88 20 32 30 31 20 22 30 34 2F 30 32 2F 37 39 22
192 20 31 35 33 34 2E 39 38 20 31 32 38 2E 36 38 20
208 22 53 41 40 45 53 20 2F 20 47 41 53 20 41 43 43
224 2E 22 00 00 60 B8 01 80 20 32 30 32 20 22 30 34
240 2F 30 33 2F 37 39 22 20 31 36 37 35 2E 35 33 20

```

FILESPEC: LEDGER

SECTOR: 6

```

0  33 2E 39 35 20 22 53 41 40 45 53 20 2F 20 50 4F
16 53 54 41 47 45 22 00 00 6E DC 01 88 20 32 30 33
32 20 22 30 34 2F 30 34 2F 37 39 22 20 31 34 37 36
48 2E 32 34 20 36 38 2E 39 38 20 22 53 41 40 45 53
64 20 2F 20 54 45 40 45 50 48 4F 4E 45 20 41 43 43
80 2E 22 00 45 6E E0 01 88 20 32 30 34 20 22 30 34
96 2F 30 35 2F 37 39 22 20 32 29 39 35 2E 37 35 20
112 31 32 31 32 2E 37 38 20 22 53 41 40 45 53 20 2F
128 20 4E 45 57 20 53 54 4F 43 4B 22 00 81 6E EA 01

```


MINI LEDGER

6AE0: 20 20 54 52 41 4E 53 41 43 54 49 4F 4E 20 44 45
 6AF0: 54 41 49 4C 53 00 2F 6B 00 00 93 20 44 45 40 45
 6B00: 54 45 20 41 4C 4C 20 27 52 45 4D 22 20 53 54 41
 6B10: 54 45 4D 45 4E 54 53 20 57 48 45 4E 20 45 41 4D
 6B20: 49 4C 49 41 52 49 53 54 49 4F 4E 20 4F 46 00 4A
 6B30: 6B 00 00 93 20 50 52 4F 47 52 41 4D 20 49 53 20
 6B40: 43 4F 4D 50 4C 45 54 45 2E 00 70 6B 00 00 0A 20
 6B50: 4C 20 33 30 29 2C 44 24 20 33 30 29 2C 43 20 33
 6B60: 30 29 2C 44 20 33 30 29 2C 45 24 20 33 30 29 00
 6B70: 00 6B 0E 00 93 20 52 45 44 55 43 45 20 4F 52 20
 6B80: 49 4E 43 52 45 41 53 45 20 54 48 45 20 4D 41 47
 6B90: 4E 49 54 55 44 45 20 4F 46 20 54 48 45 20 44 49
 6BA0: 4D 20 53 54 41 54 45 4D 45 4E 54 53 00 00 6B 00
 6BB0: 00 93 20 54 4F 20 53 55 49 54 20 52 41 4D 20 4D
 6BC0: 45 4D 4F 52 59 20 41 56 41 49 4C 41 42 4C 45 20
 6BD0: 59 4F 55 52 20 53 59 53 54 45 4D 2E 00 15 6C 02
 6BE0: 00 02 22 20 20 20 20 20 20 20 20 20 20 20 20 20
 6BF0: 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
 6C00: 20 20 54 4F 44 41 53 27 53 20 44 41 54 45 20 22
 6C10: 30 44 54 24 00 48 6C 0C 00 02 22 20 20 20 4D 20
 6C20: 49 20 4E 20 49 20 20 4C 20 45 20 44 20 47 20
 6C30: 45 20 52 20 20 20 50 20 52 20 4F 20 47 20 52 20
 6C40: 41 20 4D 20 20 20 22 00 7B 6C 00 00 02 22 20 20
 6C50: 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
 6C60: 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
 COMMAND?

6C70: 20 20 20 20 20 20 20 20 22 00 81 6C 0A 00 02
 6C80: 00 08 6C 04 01 02 20 0C 30 29 22 4C 47 52 22 30
 6C90: 0C 37 29 22 45 4E 54 52 59 22 3B 0C 31 37 29 22
 6CA0: 43 52 45 44 49 54 53 22 3B 0C 32 39 29 22 44 45
 6CB0: 42 49 54 53 22 3B 0C 34 30 29 22 54 52 41 4E 53
 6CC0: 41 43 54 49 4F 4E 22 00 0C 6D 0E 01 02 20 0C 30
 6CD0: 29 22 4E 6F 2E 22 3B 0C 37 29 22 44 41 54 45 22
 6CE0: 3B 0C 31 37 29 22 20 53 41 4C 45 53 29 22 3B 0C
 6CF0: 32 39 29 22 4F 55 54 47 4F 49 4E 47 22 3B 0C 34
 6D00: 32 29 22 44 45 54 41 49 4C 53 22 00 1D 6D 18 01
 6D10: 01 20 55 20 05 20 30 20 0D 20 36 33 00 2D 6D 22
 6D20: 01 20 20 02 20 0C 55 29 22 2D 22 3B 00 35 6D 2C
 6D30: 01 07 20 55 00 38 6D 36 01 02 00 65 6D 90 01 08
 6D40: 20 32 30 30 2C 22 30 34 2F 30 31 2F 37 39 22 2C
 6D50: 31 32 32 39 2F 37 35 2C 30 2E 30 30 2C 22 53 41
 6D60: 4C 45 53 22 00 9C 6D 0A 01 00 20 32 30 31 2C 22
 6D70: 30 34 2F 30 32 2F 37 39 22 2C 31 35 33 34 2E 39
 6D80: 30 2C 31 32 38 2E 36 38 2C 22 53 41 4C 45 53 20
 6D90: 2F 20 47 41 53 20 41 43 43 2E 22 00 0D 6D 00 01
 6DA0: 00 20 32 30 32 2C 22 30 34 2F 30 33 2F 37 39 22
 6DB0: 2C 31 36 37 35 2E 35 33 2C 33 2E 39 35 2C 22 53
 6DC0: 41 4C 45 53 20 2F 20 50 4F 53 54 41 47 45 22 00
 6DD0: 0C 6E 0C 01 00 20 32 30 33 2C 22 30 34 2F 30 34
 6DE0: 2F 37 39 22 2C 31 34 37 36 2E 32 34 2C 36 38 2E
 6DF0: 39 38 2C 22 53 41 4C 45 53 20 2F 20 54 45 4C 45
 6E00: 50 48 4F 4E 45 20 41 43 43 2E 22 00 45 6E 00 01

6E10: 00 20 32 30 34 2C 22 30 34 2F 30 35 2F 37 39 22
 6E20: 2C 32 39 39 35 2E 37 35 2C 31 32 31 32 2E 37 38
 6E30: 2C 22 53 41 4C 45 53 20 2F 20 4E 45 57 20 53 54
 6E40: 4F 43 48 22 00 01 6E 0A 01 00 20 32 30 35 2C 22
 COMMAND?

6E50: 30 34 2F 30 36 2F 37 39 22 2C 33 31 31 34 2E 31
 6E60: 36 2C 31 32 34 2E 31 38 2C 22 53 41 4C 45 53 20
 6E70: 2F 20 45 4C 45 43 54 52 49 43 20 41 43 43 2E 22
 6E80: 00 94 6E 62 02 5A 31 05 30 3A 5A 32 05 30 3A 5A
 6E90: 33 05 30 00 0A 6E 6C 02 01 20 49 20 05 20 31 20
 6EA0: 0D 20 4E 00 07 6E 76 02 20 20 08 20 4C 20 49 29
 6EB0: 2C 44 24 20 49 29 2C 43 28 49 29 2C 44 20 49 29
 6EC0: 2C 45 24 20 49 29 00 01 6F 00 02 20 20 02 20 0C
 6ED0: 30 29 38 4C 20 49 29 38 0C 37 29 38 44 24 20 49
 6EE0: 29 38 0C 31 37 29 38 43 28 49 29 38 0C 32 39 29
 6EF0: 3B 44 20 49 29 38 0C 34 30 29 38 45 24 20 49 29
 6F00: 00 12 6F 0A 02 5A 31 20 05 20 5A 31 0D 43 20 49
 6F10: 29 00 23 6F 94 02 5A 32 20 05 20 5A 32 0D 44 20
 6F20: 49 29 00 3D 6F 9E 02 5A 33 20 05 20 5A 33 0D 20
 6F30: 43 20 49 29 0E 43 20 49 29 0F 56 29 00 47 6F 00
 6F40: 02 07 20 49 3A 90 00 50 6F 02 02 01 20 55 20 05
 6F50: 20 30 20 0D 20 36 33 00 68 6F 0C 02 20 20 02 20
 6F60: 0C 55 29 22 2D 22 3B 00 70 6F 20 03 07 20 55 00
 6F70: 76 6F 2A 03 02 00 0F 6F 34 03 02 20 0F 22 54 4F
 6F80: 54 41 4C 20 44 45 42 49 54 53 20 54 48 49 53 20
 6F90: 50 45 52 49 4F 44 20 20 20 20 20 20 20 20 20 3D
 6FA0: 20 23 23 23 23 23 2E 23 23 22 3B 5A 32 00 08
 6FB0: 6F 3E 03 02 20 0F 22 54 4F 54 41 4C 20 43 52 45
 6FC0: 44 49 54 53 20 54 40 49 53 20 50 45 52 49 4F 44
 6FD0: 20 20 20 20 20 20 20 20 20 20 23 23 23 23 23 23
 6FE0: 2E 23 23 22 3B 5A 31 00 23 70 48 03 02 20 0F 22
 6FF0: 54 4F 54 41 4C 20 56 41 54 20 4F 4E 20 53 41 4C
 7000: 45 53 20 54 49 49 53 20 50 45 52 49 4F 44 20 20
 7010: 20 3D 20 23 23 23 23 23 23 2E 23 23 22 3B 5A 31
 7020: 0F 56 00 5C 70 52 03 02 20 0F 22 4E 45 54 20 43
 COMMAND?

7030: 52 45 44 49 54 20 20 20 4C 45 53 53 20 56 41 54
 7040: 29 20 20 20 20 20 20 20 20 20 20 20 20 20 22 23
 7050: 23 23 23 23 2E 23 23 22 3B 5A 33 00 94 70 5C 03
 7060: 02 20 0F 22 43 52 45 44 49 54 20 42 41 4C 41 4E
 7070: 43 45 20 42 52 4F 55 47 48 54 20 46 4F 52 57 41
 7080: 52 44 20 20 20 30 20 23 23 23 23 23 2E 23 23 23
 7090: 22 3B 50 00 02 70 66 03 02 20 0F 22 43 52 45 44
 70A0: 49 54 53 20 20 4C 45 53 53 20 41 42 4F 56 45 20
 70B0: 44 45 42 49 54 53 29 20 43 2F 46 20 20 30 20 23
 70C0: 23 23 23 23 23 2E 23 23 22 3B 50 0D 5A 33 0E 5A
 70D0: 32 00 03 70 70 03 01 20 55 20 05 20 30 20 0D 20
 70E0: 36 33 00 03 70 70 03 20 20 02 20 0C 55 29 22 3D
 70F0: 22 3B 00 0B 70 04 03 07 20 55 00 01 71 07 03 00
 7100: 00 00 00 05 05 05 05 05 05 05 05 05 05 05 05 05
 7110: 05 05 05 05 05 05 05 05 05 05 05 05 05 05 05 05

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CC SOFT	65
CHROMASONICS	12
COMP, COMP, COMP	74 & 75
CROFTON	36
DIRECT DATA MARKETING	6
ELECTRONIC BROKERS	53
GP INDUSTRIAL	65
HAL COMPUTERS	6
HAPPY MEMORIES	8
HENRYS	39
INKRAFT	53
LOTUS SOUND	48 & 66
LP ENTERPRISES	4
NEWBEAR	76
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NASCOM 1 with 3 amp power supply, built but unused, auto cassette drive, £150.00. 15 Station Road, Weaverham, Northwich, Cheshire, or Tel: Weaverham 852722.

TRS-80, 16K level 11 complete system. £620. Phone Stafford 822828.

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16K Static Memory Board	£282.00	£306.00
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LYNTON S-100 6 connector Mother Board		£87.00
LYNTON S-100 Mother Board and Power Supply		£175.00
LYNTON S-100 Mother Board, Power Supply cased		£232.00

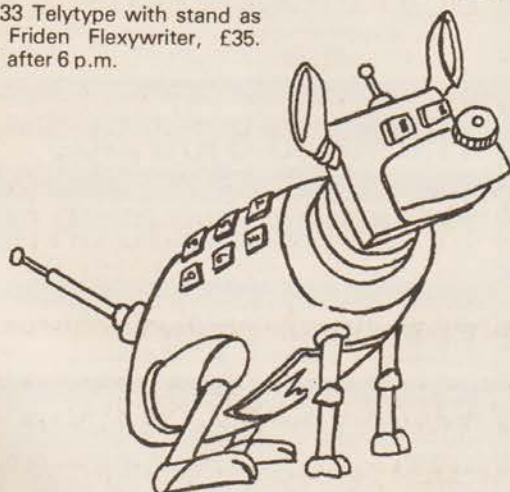
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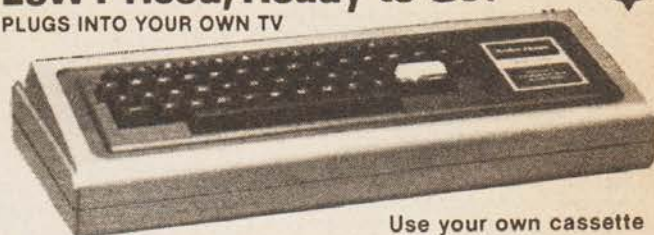
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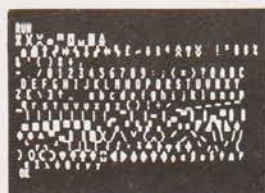
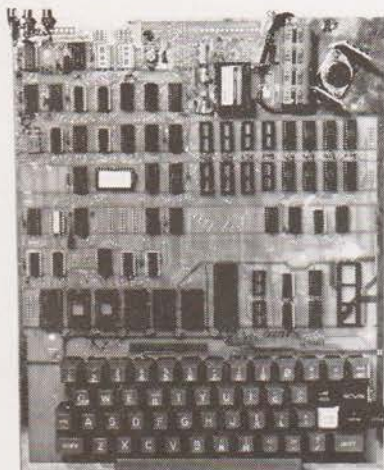
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LOG(X) POS(I) RND(X) SGN(X) SIN(X)
SPC(I) SQR(I) TAB(I) TAN(X) USR(I)

STRING FUNCTIONS
ASC(X\$) CHR\$(I) FRE(X\$) LEFT\$(X\$,I) LEN(X\$) MID\$(X\$,I,J)
RIGHT\$(X\$,I) STR\$(X)

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FULL CONSTRUCTION DETAILS
IN P.E. AUG 1979 EDITION

Delivery date June 1979
at the 1979 MicroComputer Show
Customer orders in strict rotation only.

COMMANDS
CONT LIST NEW NULL RUN
STATEMENTS
CLEAR DATA DEF DIM END FOR
GOTO GOSUB IF, GOTO IF, THEN INPUT LET
NEXT ON, GOTO ON, GOSUB POKE PRINT READ
REM RESTORE RETURN STOP

EXPRESSIONS
OPERATORS
+ * / ^ NOT AND OR > < <> >=<= RANGE 10⁻³² to 10⁺³²

VARIABLES
A, B, C, ... Z and two letter variables
The above can all be subscripted when used in an array. String variables use above names plus \$, e.g. A\$.
FUNCTIONS



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- @ Erases line being typed, then provides carriage return, line feed.
- ␣ Erases last character typed.
- CR Carriage Return — must be at the end of each line.
- | Separates statements on a line.
- CONTROL/C Execution or printing of a list is interrupted at the end of a line.
- "BREAK IN LINE XXXX" is printed, indicating line number of next statement to be executed or printed.
- CONTROL/O No outputs occur until return made to command mode. If an Input statement is encountered, either another CONTROL/O is typed, or an error occurs.
- ? Equivalent to PRINT

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